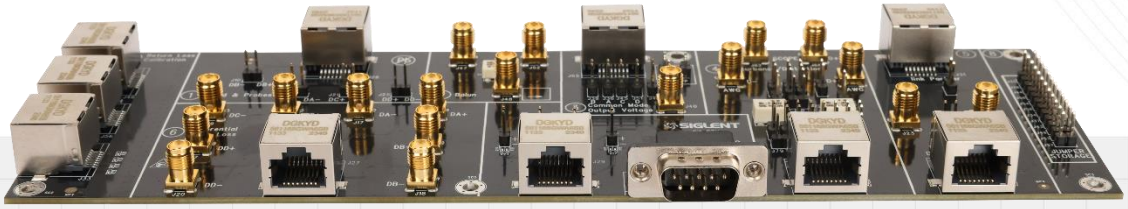
100 BASE-TX Ethernet Compliance Test Application

User Manual

EN01A



SIGLENT TECHNOLOGIES CO.,LTD

Contents

1 Introduction

Siglent provides 100 BASE-TX and 1000 BASE-T Ethernet Compliance Test application to verify the Ethernet transmitter device under test (DUT) compliance to specifications. The equipment required for Ethernet conformance testing including Siglent SDS7000A oscilloscope, Vector Network Analyzers, test fixture, probes, Arbitrary Waveform Generator and Ethernet Compliance Test Application software. This user manual only introduces the test fixture, test methods and connection for 100 BASE-TX Ethernet Compliance Test.

The Ethernet Compliance Test Application:

- Let's you select individual or multiple tests to run.
- Shows you how to connect the oscilloscope to the device under test (DUT).
- Automatically sets up the oscilloscope for every test project.
- Provides detailed information for every test that has been run, and lets you know the thresholds at which marginal or critical warnings appear.
- Creates HTML or XML test reports of the tests that have been run.

2 Test Items and Standards Reference

2.1 Test Items

Siglent's SDS7000A Oscilloscope and Ethernet Compliance Test Fixture supports the following 100 BASE-TX Ethernet Electrical Compliance Test items:

- Template Tests
- Amplitude Domain
  - Peak Voltage Tests
  - Amplitude Symmetry Tests
  - Overshoot Tests
- Time Domain
  - Rise and Fall Time Tests
  - Rise and Fall Time Symmetry Tests
- Duty Cycle Distortion Tests
- Transmitter Jitter Tests
- MDI Return Loss
  - Transmitter Return Loss Tests
  - Receiver Return Loss Tests

2.2 Standards Reference

Siglent provides the 100 BASE-TX Ethernet Compliance Test solution which follows the IEEE802.3u and ANSI X3.263-1995 standards, and Table 2-1 shows the standard for every test item.
More information for the IEEE802.3 standard, please go to the website: www.ieee802.org.

Table 2-1 100 BASE-TX Test by Standard Reference

Standard Reference	Description
ANSI X3.263-1995，Annex J	UTP AOI (Active Output Interface) template
ANSI X3.263-1995，Section 9.1.2.2	UTP +Vout Differential voltage
ANSI X3.263-1995，Section 9.1.2.2	UTP -Vout Differential voltage
ANSI X3.263-1995，Section 9.1.4	Signal amplitude symmetry
ANSI X3.263-1995，Section 9.1.3	+Vout overshoot
ANSI X3.263-1995，Section 9.1.3	-Vout overshoot
ANSI X3.263-1995，Section 9.1.8	Duty cycle distortion
ANSI X3.263-1995，Section 9.1.9	Transmitter jitter
ANSI X3.263-1995，Section 9.1.6	AOI +Vout rise time
ANSI X3.263-1995，Section 9.1.6	AOI +Vout fall time
ANSI X3.263-1995，Section 9.1.6	AOI +Vout rise/fall time symmetry
ANSI X3.263-1995，Section 9.1.6	AOI -Vout rise time
ANSI X3.263-1995，Section 9.1.6	AOI -Vout fall time
ANSI X3.263-1995，Section 9.1.6	AOI -Vout rise/fall time symmetry
ANSI X3.263-1995，Section 9.1.5	Transmitter return loss
ANSI X3.263-1995，Section 9.2.2	Receiver return loss

3 Test equipment

3.1 Required Equipment

The Ethernet electrical compliance test measurements require the following equipment:

- Oscilloscope (SDS7000A): Oscilloscope's bandwidth larger than 2GHz, and with the Ethernet Compliance Test Application software that has installed the option key (SDS7000A-CT-100BASE-T option for 100 BASE-TX, SDS7000A-CT-1000BASE-T option for 1000BASE-T).
- FX-ETH kit: FX-ETH kit is the Ethernet Electrical Compliance Test Fixture from Siglent that provides the physical connection and test points after the DUT enters into the test mode.
- Differential probe or SMA cables:
  - Differential probe (e.g., SAP2500D or SAP5000D): bandwidth greater than 2 GHz for probing signals;
  - SMA cables: connects from the oscilloscope to the test fixture for probing signals.
- Vector Network Analyzer: VNA is used for MDI return loss test.
- USB Connection Cable: The cable is used to connect the USB Host port on the oscilloscope to the USB Device port on the network analyzer, so that the oscilloscope can control and configure the network analyzer and obtain the return loss test data.
- Arbitrary waveform generator: On the 1000BASE-T compliance tests, when the DUT enters Test Mode 1 or Test Mode 4, for the Peak Output Voltage tests, Template tests, Droop tests, Transmitter Distortion tests with disturbing signal, a dual- channels arbitrary waveform generator which outputs the required disturbing signals.
- Jitter test cable: On the 1000BASE-T compliance tests, when the DUT enters Slave mode, for the jitter tests with TX_TCLK, a 103m long cable is required to connect the DUT to the Link Partner.

3.2 Delivery Checklist

The FX-ETH kit includes the items listed in Table 3-1. When you receive the FX-ETH, firstly, verify that all items listed on the checklist have been received. If you notice any omissions or damage, please contact your nearest Siglent customer service center or distributor as soon as possible. If you fail to contact us immediately in case of omissions or damage, we will not be responsible for replacement.

Table 3-1 FX-ETH Kit Checklist

Item name	Quantities
User Manual	1
Test Fixture Board	1
UTP RJ45 Cable（6 inches）	1
50Ω Terminators（SMA）	8
SMA cables	4
BNC-SMA Adaptors	4
Jumpers	12

3.3 Introduction to FX-ETH Test Fixture

FX-ETH kit is the Ethernet Electrical Compliance Test Fixture which cooperates with software for 100 BASE-TX and 1000 BASE-T ethernet compliance validation on SDS7000A.

The test fixture board shown in Figure 3-1 which consists of 9 sections, every section has some specific functions, which are clearly marked on the board to help user to use the test fixture.

Figure 3-1 Ethernet Electrical Compliance Test Fixture Board

Every section on the board is described as follows:

Section 0: Return loss calibration section. The vector network analyzer can be calibrated for Open, Short, and Load when DUT runs return loss tests.

Section 1: Supports most of the Ethernet Compliance tests for 100 BASE-TX and 1000 BASE-T by using a differential probe.

Section 2: Differential to single-ended signal conversion by using a balun, which supports return loss tests by using one Port on the VNA.

Section 3: Supports for 1000 BASE-T MDI common-mode output voltage tests.

Section 4: Supports Test Mode 1 and Test Mode 4 on 1000Base-T compliance tests with disturbing signals.

Section 5: Under 100 BASE-TX compliance tests, the Link Partner such as the SDS7000A oscilloscope transmits at 100Mbps. The DUT transmitter should then emit the following waveform to support the compliance tests.

Section 6: Supports most of the Ethernet Compliance tests for 100 BASE-TX and 1000 BASE-T by using two SMA cables.

Section 7: Supports 1000 BASE-T jitter tests.

Section 8: Jumper storage section, which can store 12 jumpers.

4 Compliance Test Software

Siglent's 100 BASE-TX Ethernet Compliance Test is a solution based on IEEE802.3u and ANSI X3.263-1995 specifications. The Ethernet Compliance analysis software controls the oscilloscope to automatically perform the tests. The graphical operation guide simplifies the measurement process, the test items can be flexibly configured, and the test report records the entire measurement results, including the test values and the screenshots of the test waveforms.

SDS7000A provides 100 BASE-TX Compliance Test function, according to **Analysis** -> **Compliance Test** -> **Protocol Type** , select **100 BASE-TX** and click **ON** to activate the Compliance Test function, which are shown in Figure 4-1. The Compliance Test function is divided into three main parts: **Test Config** , **Results** , and **Report Setting** .

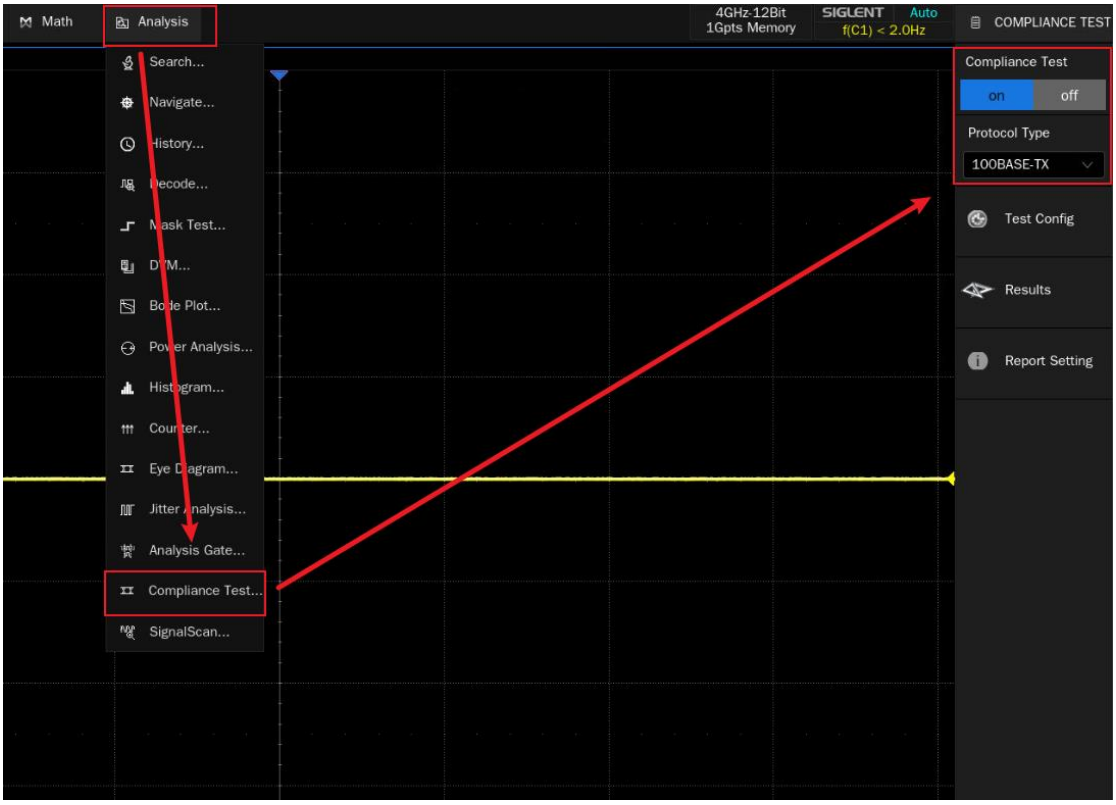


Figure 4-1 Launching 100 BASE-TX Compliance Analysis Software

4.1 Test Configuration

Clicking on **Test Config** will pop up the specific test configuration window, as shown in Figure 4-2, which is divided into six steps based on the test process: **Setup** , **Test Select** , **Configure** , **Connect** , **Run Test** , and **Result** .

➢ **Setup:**

1) Provide the functions of " **Recall** ", " **Last** " and " **Save** " for the configuration.
2) In " **Link Partner Select** ", select the Link Partner device to obtain the scrambled / idle / sequence for 100 BASE-TX tests. You can either select **Use Other Devices** or **Use SDS7000A Series Scope** as the Link Partner.

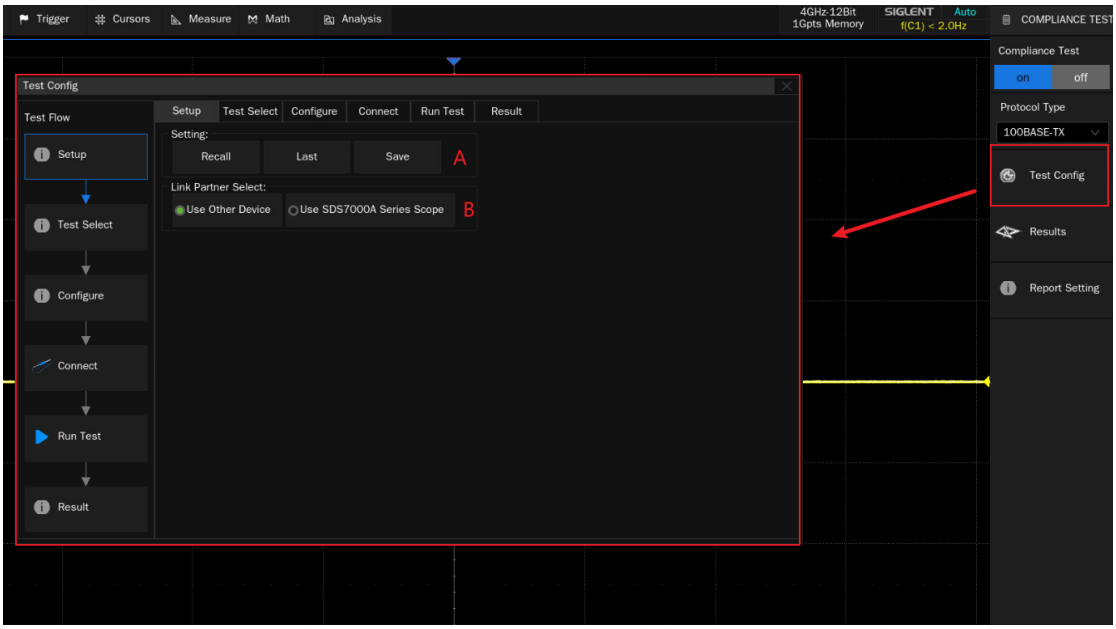


Figure 4-2 Test Configuration Window

➢ **Test Select:** Select the items to be tested in this column, as shown in Figure 4-3.

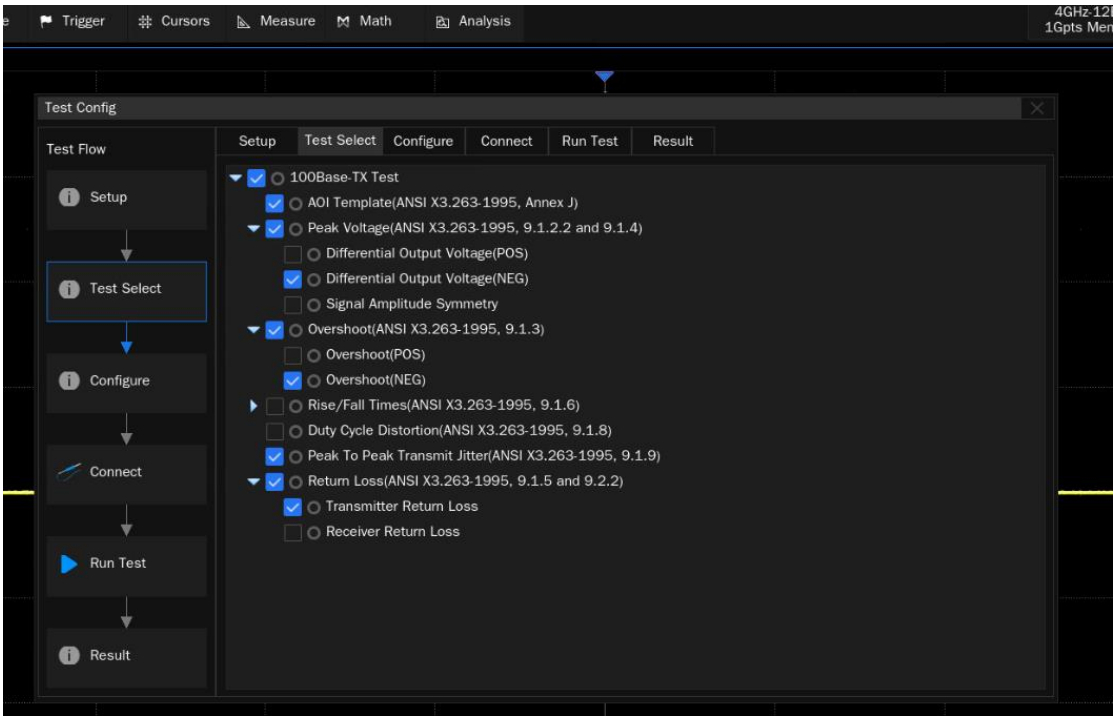


Figure 4-3 Test Item Selection Window

- **Configure:** The test items selected in **Test Select** will be highlighted in this column, and you can click the corresponding items to configure. You can set the input channels and probe type, as shown in Figure 4-4. And the pulse width has two options, which are 80ns and 96ns, as shown in Figure 4-5.

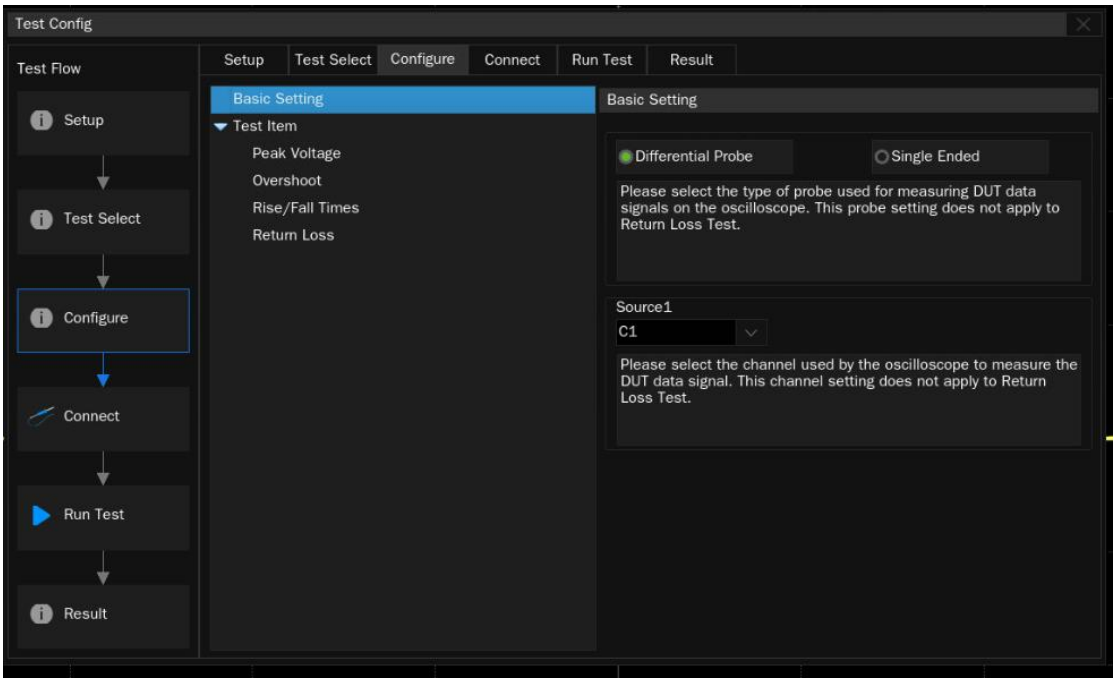


Figure 4-4 Configuration Window

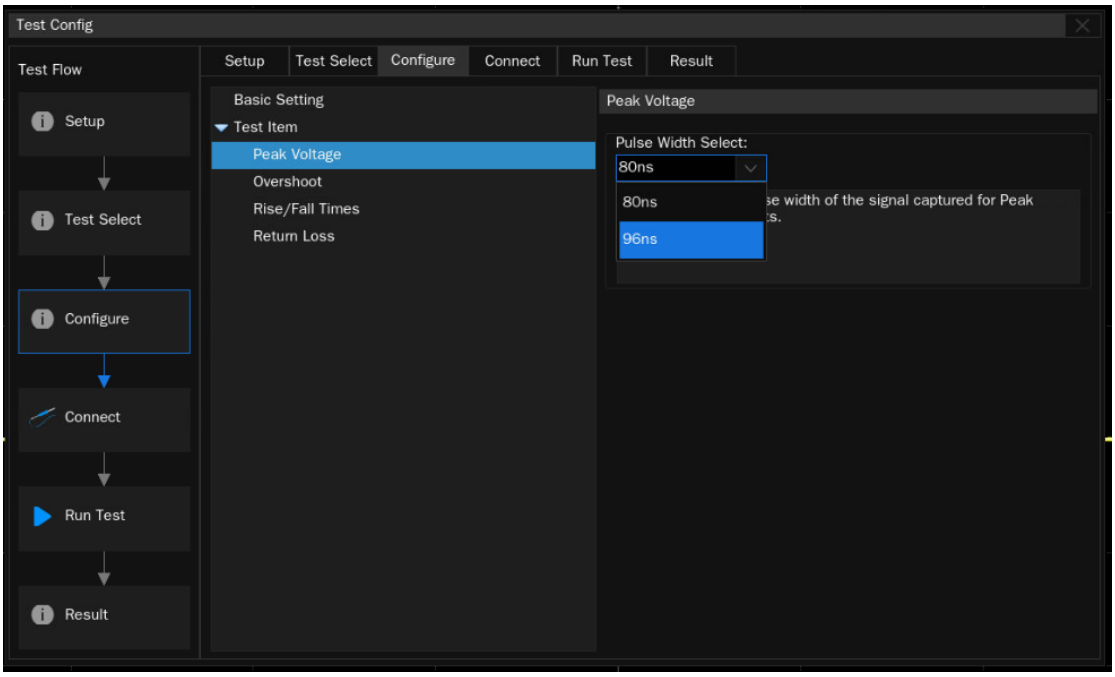


Figure 4-5 Pulse Width of the DUT

- **Connect:** This column displays the connection diagram of the compliance test, as shown in Figure 4-6. If more than one item is selected simultaneous, only the connection diagram for the first test item will be displayed. For the other test items, if the connection is different then a new pop-up window will appear at the end of the previous test.

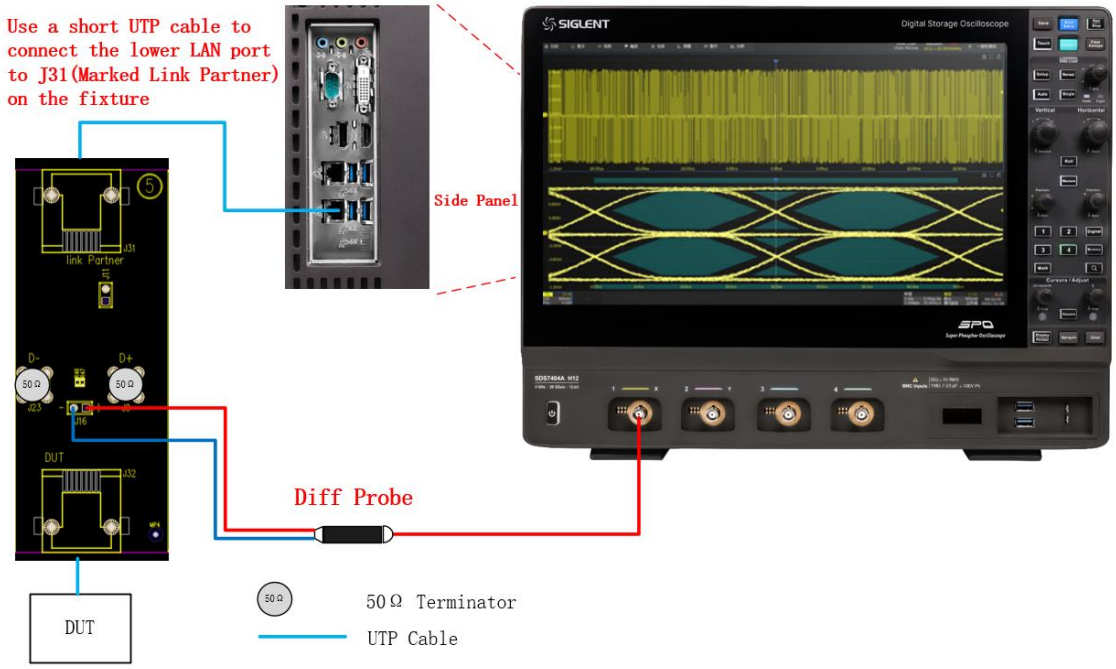


Figure 4-6 Connection Diagram in the Connect Menu

- **Run test:** The Run Test window is shown in Figure 4-7. Both " **Continue** " and " **Stop** " options are supported when meets test failures.

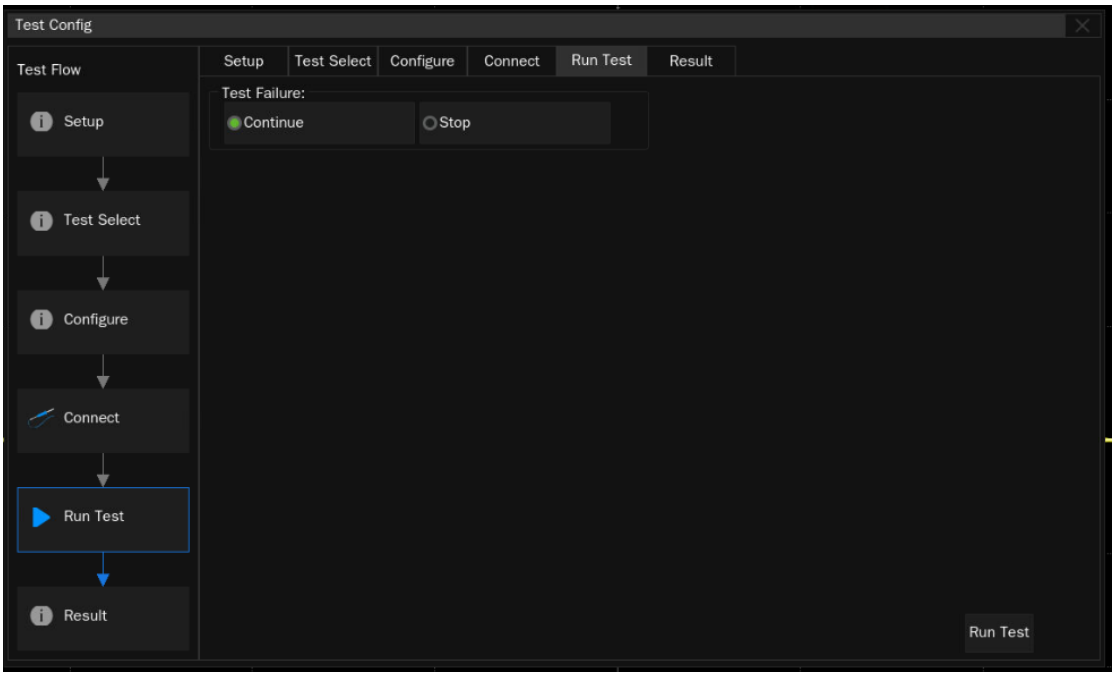


Figure 4-7 Run Test Window

In the following test process, according to the pop-up window prompts to complete the test. After all test items are completed, the test result window will pop up.

4.2 Viewing of Results

Click " **Result** " to view the corresponding test results.

The upper half of the test results window contains the test items, outlining the results of every test item, as well as the pass thresholds, as shown in Figure 4-8.

The lower half of the test result window is the corresponding detail picture, click on the item you concern in the upper half of the test results window, and the corresponding details will be displayed in the lower half of the window, click on the picture to see the details of the test waveform in large view, as shown in Figure 4-9.

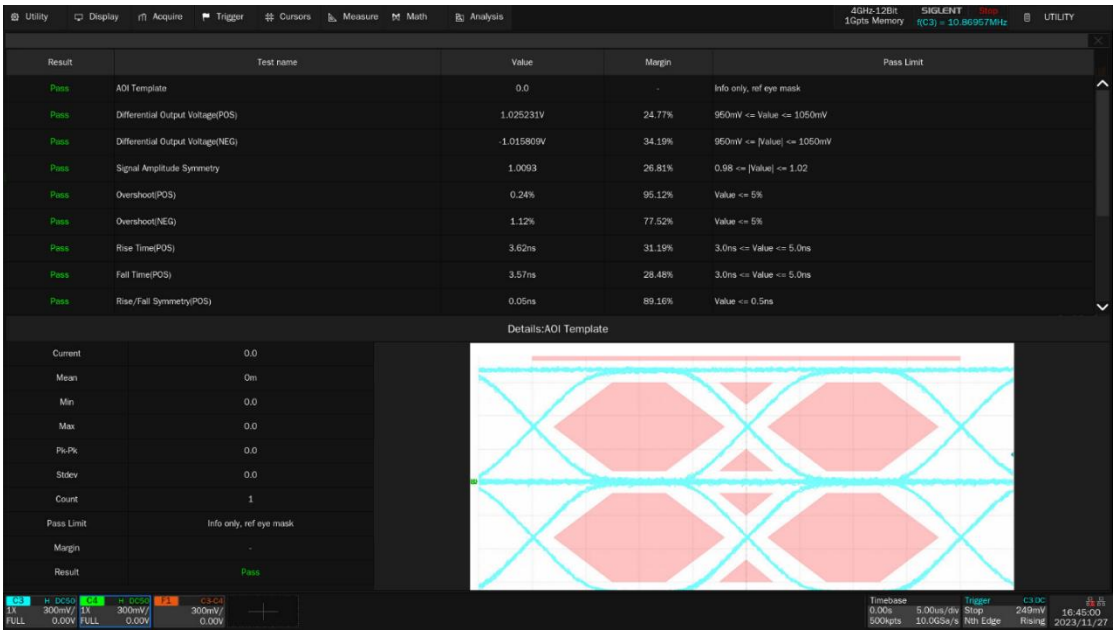


Figure 4-8 List of Test Result Items

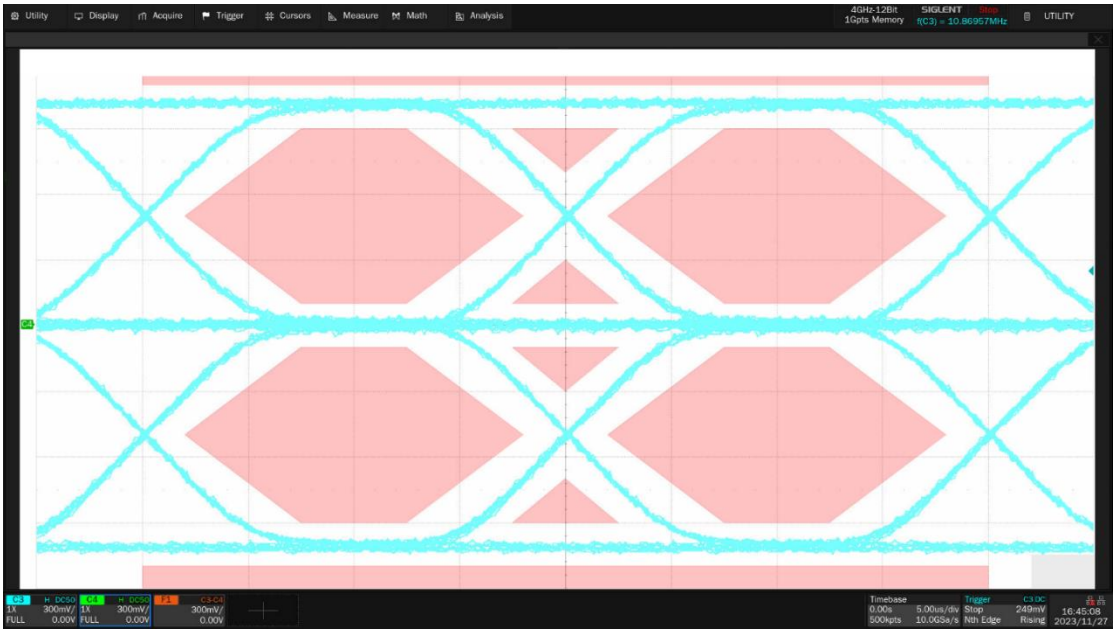


Figure 4-9 Waveform Details

4.3 Report Generation

Click **Report Setting** , fill in the test information, and select the HTML or XML report type. **Preview Report** can view the generated report in advance. Click **File Management** to select the path to save. Click **Save** to save the test results, as shown in Figure 4-10.

Note: When saved in HTML format, a folder and HTML files will be generated, if you need to copy to a new directory, you need to copy both to the new directory.

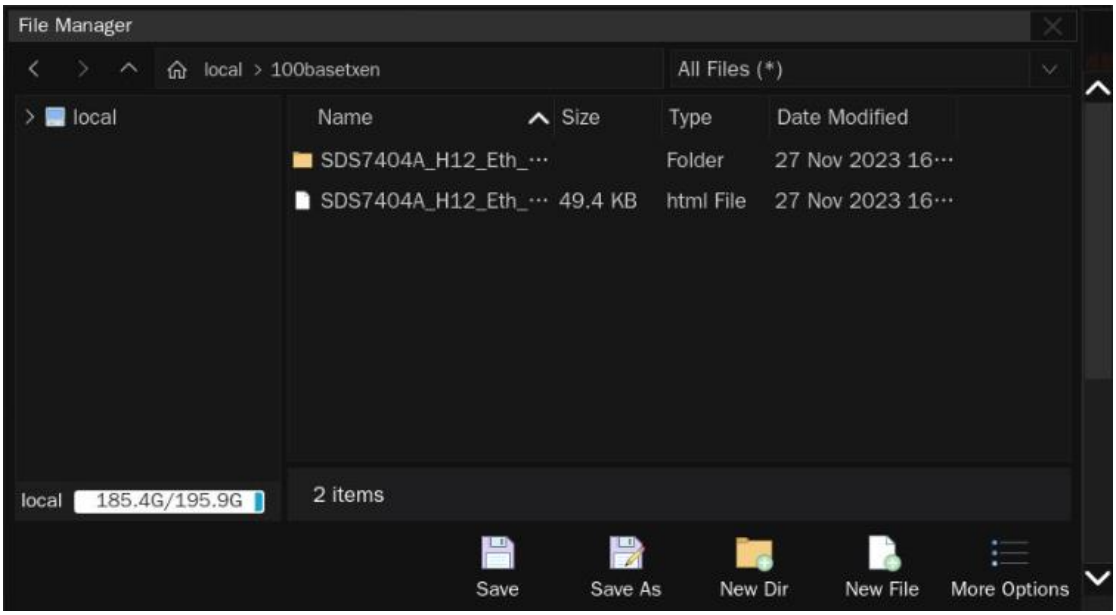


Figure 4-10 Generation of Report Settings

The test report includes a summary table of all test results with hyperlinks to the details page, which includes a screen shot of the associated test waveform, which is shown in Figure 4-11.

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ETH Compliance Test Reoprt

Overall Result: Pass

Operator:	Milton
Test Date:	2024-02-29 14:59:40
Device:	TI Demo
Temperature:	23
Remarks:	100 Base-TX compliance test
Oscilloscope Name:	SDS7404A H12
Oscilloscope Serial Number:	SDS70020230506
Oscilloscope Scope ID:	dd08-24b9-01db-4286
Oscilloscope Firmware Version:	04.13.01.1.1.5.0_rca00
Test Result:	Total:15,Pass:15,Not Tested:0,Fail:0

Summary

RESULT	TEST ITEM	VALUE	VAL(MIN)	VAL(MAX)	MARGIN	LIMIT
PASS	PEAK_VOLTAGE_POS	1.024762V	1.024762V	1.024762V	25.24%	950mV <= Value <= 1050mV
PASS	PEAK_VOLTAGE_NEG	-1.0369688V	-1.0369688V	-1.0369688V	13.01%	950mV <= |Value| <= 1050mV
PASS	PEAK_VOLTAGE_SYMMETRY	0.9882	0.9882	0.9882	79.46%	0.98 < |Value| < 1.02
PASS	A01_TEMPLATE_MASK_TEST	0.00	0.00	0.00	-	Info only, ref eye mask
PASS	OVERSHOOT_POS	0.24%	0.24%	0.24%	95.20%	Value <= 5%
PASS	OVERSHOOT_NEG	-0.35%	-0.35%	-0.35%	106.94%	Value <= 5%
PASS	RISE_TIME_POS	3.82ns	3.82ns	3.82ns	40.88%	3.0ns <= Value <= 5.0ns
PASS	FALL_TIME_POS	3.67ns	3.67ns	3.67ns	33.37%	3.0ns <= Value <= 5.0ns
PASS	RF_TIME_SYMMETRY_POS	0.15ns	0.15ns	0.15ns	70.73%	Value <= 0.5ns
PASS	RISE_TIME_NEG	4.01ns	4.01ns	4.01ns	49.30%	3.0ns <= Value <= 5.0ns
PASS	FALL_TIME_NEG	3.90ns	3.90ns	3.90ns	45.02%	3.0ns <= Value <= 5.0ns
PASS	RF_TIME_SYMMETRY_NEG	0.11ns	0.11ns	0.11ns	77.28%	Value <= 0.5ns
PASS	RF_TIME_SYMMETRY	0.34ns	0.34ns	0.34ns	31.45%	Value <= 0.5ns
PASS	DUTY_CYCLE_TOTAL	0.14ns	0.14ns	0.14ns	72.90%	Value <= 0.5ns
PASS	JITTER_TOTAL	0.43ns	-0.22ns	0.20ns	69.56%	Value <= 1.4ns

Details

A01_TEMPLATE_MASK_TEST	
Current	0.00
Mean	0.0m
Min	0.00
Max	0.00
Pk-Pk	0.00
Stdev	0.00
Count	1
Pass Limit	Info only, ref eye mask
Margin	-
Result	PASS

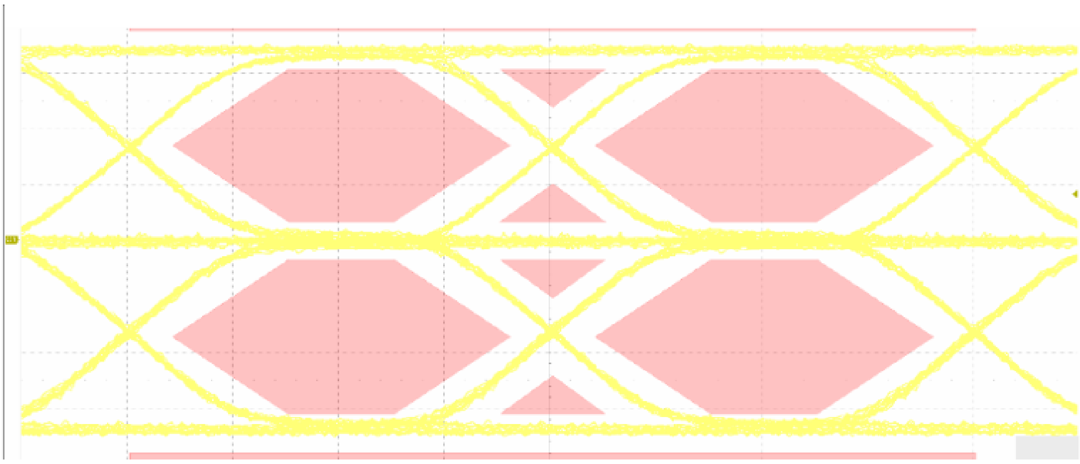

Figure 4-11 Test Report

5 100 BASE-TX Test Environment and Connectivity

The IEEE802.3u specification specifies the waveform requirement for 100 BASE-TX compliance test. The DUT is required to provide scrambled, MLT-3 encoded / idle / code-groups (this is a 3-level pseudo-random bit sequence).

If you are using another 100 BASE-TX device (Link Partner) for the test pattern generation, then the SDS7000A Oscilloscope can act as a Link Partner.

If your device does not require a link partner, please see “5.1 Probing for 100 BASE-TX Tests, Without Link Partner”. Otherwise, if your device does require a link partner, please see “5.2 Probing for 100 BASE-TX Tests, With Link Partner ”.

5.1 Probing for 100 BASE-TX Tests, Without Link Partner

When performing the 100 BASE-TX tests without a link partner, the user can use packet sending tool or modify the registers to let the DUT output the required test pattern for 100 BASE-TX compliance tests.

5.1.1 Use SMA Cables to Probe Signal

SMA cables connection is as shown in Figure 5-1.

1) Connect the DUT to the J27 connector on section ⑥ of the test fixture by using a short UTP cable.
2) Connect the test points J17(DA-) and J4(DA+) on section ⑥ of the test fixture to two input channels on the oscilloscope by using two SMA cables.
3) Connect other unused test points on section ⑥ of the test fixture to 50Ω terminators.

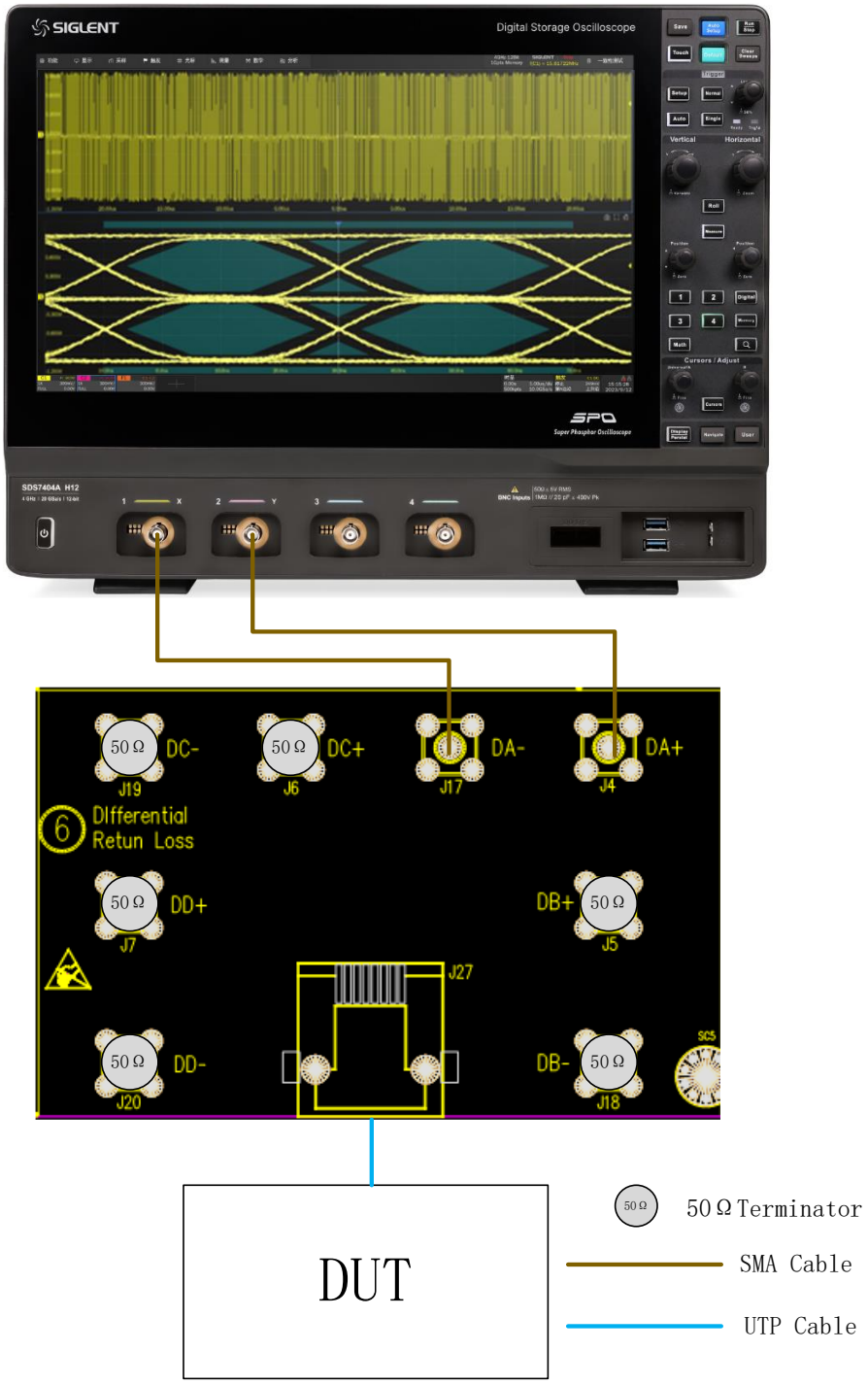

Figure 5-1 Connectivity for 100 BASE-TX Tests with SMA Cables, Without Link Partner

5.1.2 Use a Differential Probe to Probe Signal

Connectivity by using a differential probe for 100 BASE-TX tests is shown as Figure 5-2.

1) Connect the DUT to the J28 connector on section ① of the test fixture by using a short UTP cable;
2) Connect a differential probe to test point J1 (DA+,DA-) on section ① of the test fixture, and to the configured input channel of the oscilloscope.
3) Ensure correct polarity of the probe head.

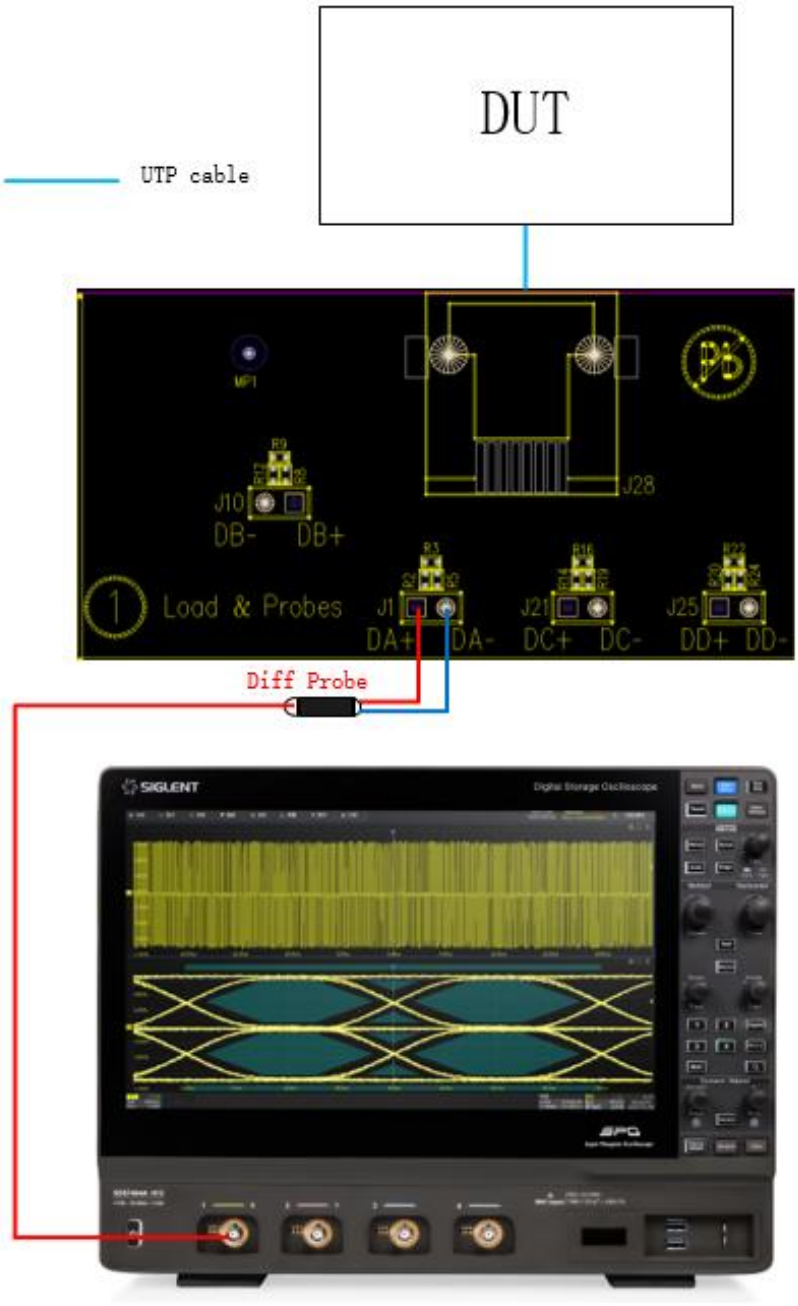

Figure 5-2 Probing for 100 BASE-TX Compliance Tests with a Differential Probe, Without Link Partner

5.2 Probing for 100 BASE-TX Tests, With Link Partner

When the user uses packet sending tool or modify the registers to let the DUT output the required test pattern for 100 BASE-TX compliance tests. The tool may have an intuitive interface, but its application has some obvious limitations. When the DUT cannot run DOS or Windows system, or if the tester is not convenient to configure the DUT to enter the test mode, it cannot control the DUT to send the require test pattern. In this case, it is necessary to use a simple method to let the DUT provide the required test pattern to support the compliance test.

The induced packet for sending is using the 100 BASE-TX self-negotiation mode, which requires a Link Partner device. Firstly, configure the Link partner's network card to 100MHz full/half-duplex mode, or send 100M idle mode waveforms actively, and then connect the TX signal on transmitter side (Link Partner) to the RX (DUT's receiver) signal. When the DUT receives the 100M idle mode waveform, it will return the same waveform. Then, the user can connect the TX signal on DUT to the test fixture. The connection and configuration figure is shown in Figure 5-3.

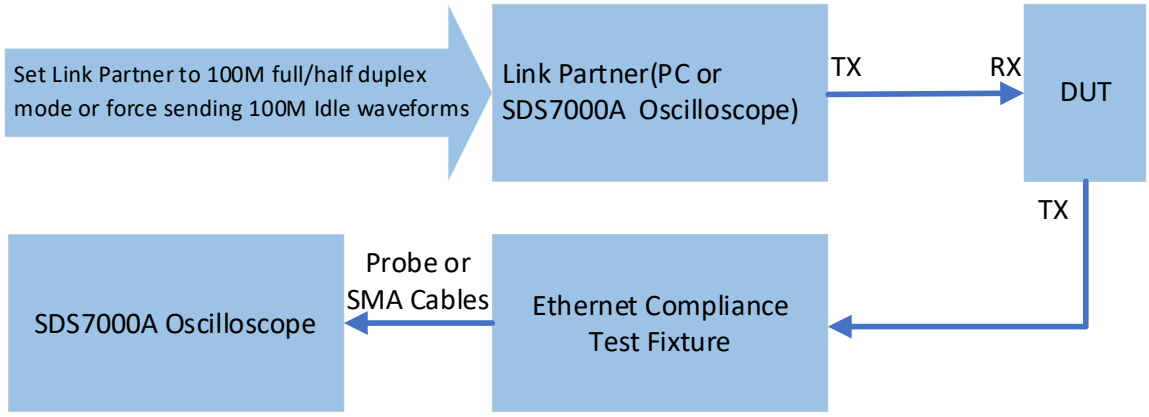

Figure 5-3 Connection for Link Partner to Induce DUT to Send Test Pattern

In the SDS7000A Ethernet Compliance Test software, in order to facilitate the user to configure the DUT to send out scrambled, MLT-3 encoded / idle / code-groups, the user can set the SDS7000A oscilloscope as the Link Partner, and connect the lower ethernet port on the SDS7000A oscilloscope to the DUT. The setup order is **Link Partner Select:** -> **Use SDS7000A Series Scope** , as shown in Figure 5-4.

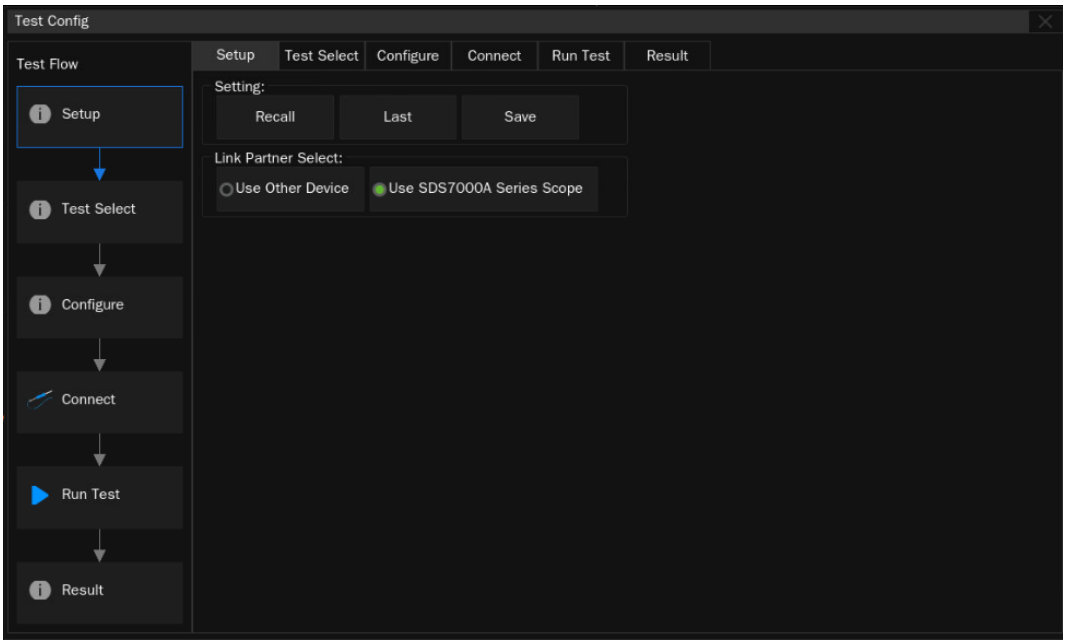

Figure 5-4 Support SDS7000A Scope as the Link Partner

When the connection is successfully, we can easily observe the test waveform from the DUT on the oscilloscope screen, which contains all the test waveforms required for the 100 BASE-TX compliance tests. During the test, the 100 BASE-TX analysis software will control the SDS7000A oscilloscope to automatically set the appropriate trigger mode to capture and analyze the waveform.

Choose the SDS7000A oscilloscope as the Link Partner, which also supports SMA cables or differential probe to probe signals.

5.2.1 Use SMA Cables to Probe Signal

The setup environment by using the SMA cables is shown as Figure 5-5. The test procedure is as follows:

1. In the **Test Config** -> **Setup** label, in the **Link Partner Select** tag, select **Use SDS7000A Series Scope** as the Link Partner.
2. Connect the DUT to the J32 connector on section ⑤ of the test fixture by using a short UTP cable.
3. Connect the lower LAN port on the SDS7000A Scope to the J31 connector (marked Link Partner) on the section ⑤ of the test fixture by using another UTP cable.
4. Connect the J23(D-) and J8(D+) connectors on section ⑤ of the test fixture to two input channels on the oscilloscope by using two SMA cables.

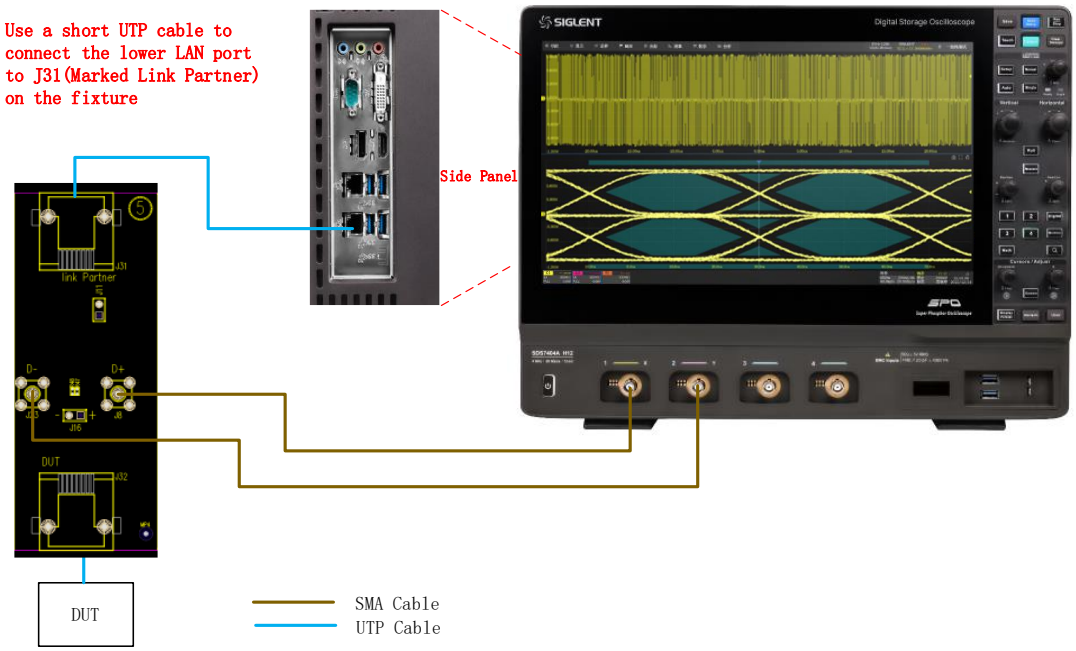

Figure 5-5 Using the SDS7000A Scope to as the Link Partner, with SMA Cables Connection

5.2.2 Use a Differential Probe to Probe Signal

The setup environment by using a differential probe is shown in Figure 5-6. The test procedure is as follows:

1) In the **Test Config** -> **Setup** label, in the **Link Partner Select** tag, select **Use SDS7000A Series Scope** as the Link Partner.
2) Connect the DUT to the J32 connector on section ⑤ of the test fixture by using a short UTP cable.
3) Connect the lower LAN port on the SDS7000A Scope to the J31 connector (marked Link Partner) on the section ⑤ of the test fixture by using another UTP cable.
4) Connect two 50Ω terminators to J23 (D-) and J8 (D+) to do the 100Ω termination for the DUT's TX signal pair.
5) Connect a differential probe to test point J16 (DA+,DA-) on section ⑤ of the test fixture, and to the configured input channel of the oscilloscope.
6) Ensure correct polarity of the probe head.

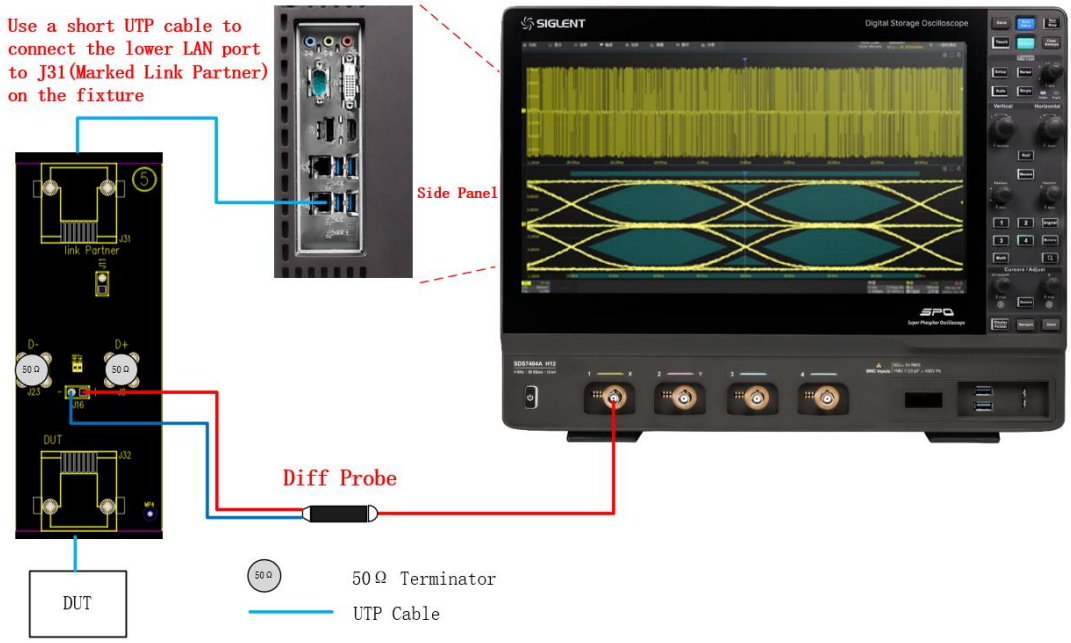

Figure 5-6 Use SDS7000A Scope as the Link Partner, with a Differential Probe Connection

6 Test procedure and test results for reference

6.1 Template Tests

Twisted pair Active Output Interface template testing helps user to understand potential signal quality issues and verify whether the transmitter signal meets the requirements for various items such as jitter, overshoot, rise time, and fall time in the IEEE standard. The template is defined in Annex J of the ANSI X3.263-1995 standard and a 5% geometric tolerance of the template is specified， as shown in Figure 6-1.

To complete this test, the device under test (DUT) is configured for 100 BASE-TX operation, and DUT sends scrambled, MLT-3 encoded /idle/ code-groups (this is a 3-level pseudo-random bit sequence).

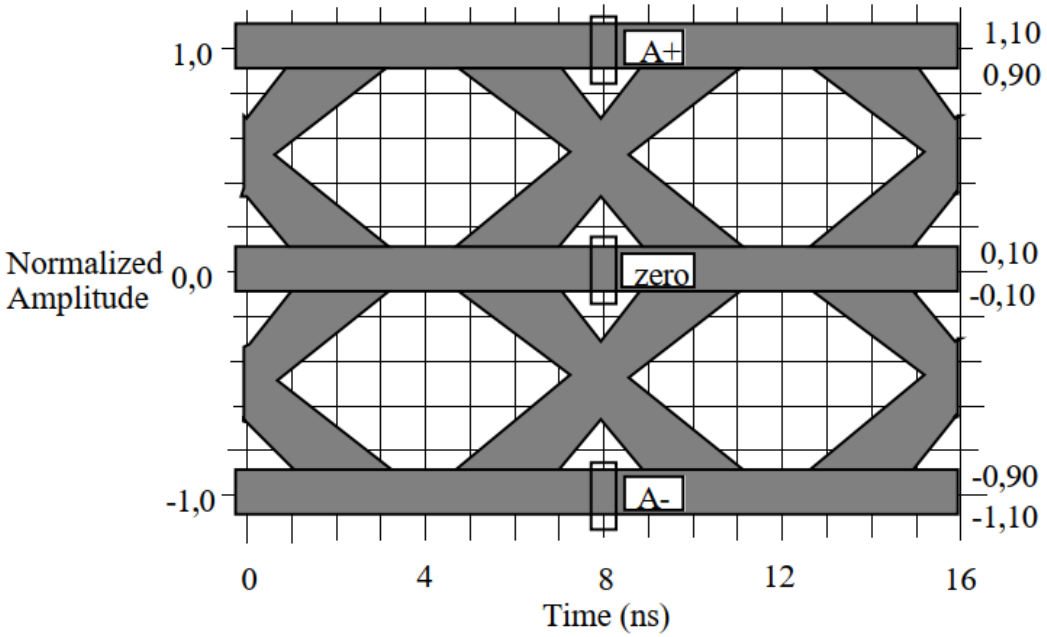

Figure 6-1 Twisted Pair AOI Templates

6.1.1 Test Procedure

1) Select **AOI Template (ANSI X3.263-1995, Annex J)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded / idle / code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test**.
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT “Source” channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test results.

6.1.2 Algorithm

The ANSI X3.263-1995 specification does not require this test. It is provided for informative purposes. The template is first centered vertically on the eye pattern baseline. It is then translated horizontally and scaled in amplitude for the best fit to the eye pattern. The scaling range is limited to the range specified in ANSI X3.263-1995 (0.95 and 1.05 for UTP).

Once the mask is aligned with the signal, the software analyzes the top portion of the mask, which reduces the effect of vertical noise errors on the measurement. During the test, the program identifies the number of waveforms captured, where every waveform is tested against the mask. The total number of failures for the top half of the mask is recorded.

Repeat the process for the bottom half of the mask and recording the number of failures at the bottom. Report the total number of failures. Although it is not in the compliance requirements, ideally the total number of failures should be zero.

6.1.3 Test Results Reference

The AOI template test results are shown in Figure 6-2.

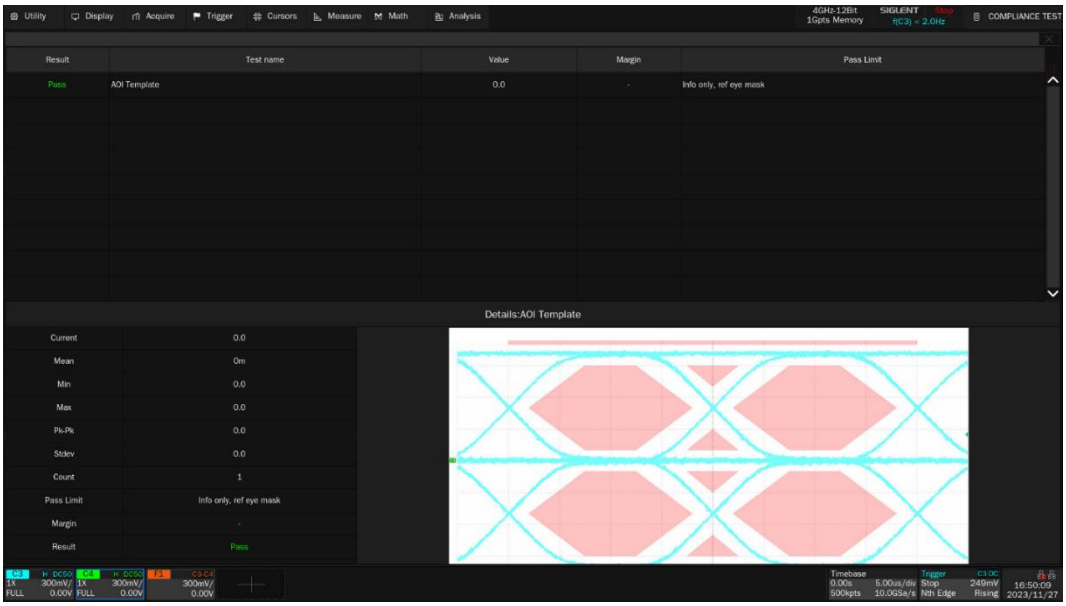

Figure 6-2 Template Test Results

Figure 6-3 shows the details of the test waveform.

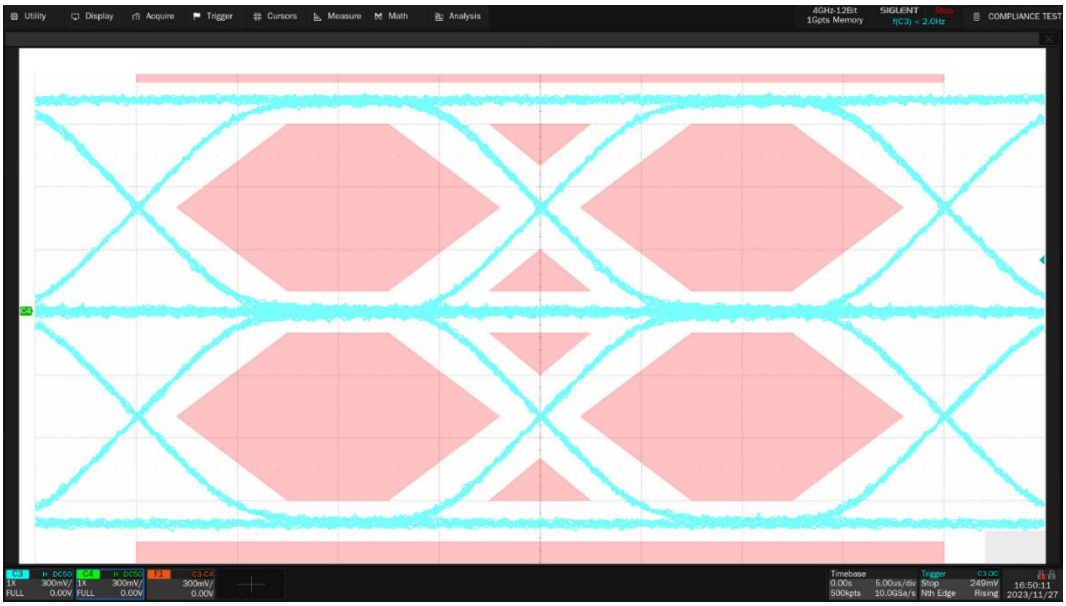

Figure 6-3 Details of the Template Test Waveform

6.2 Peak Voltage Tests

The peak voltage tests are including the differential output voltage tests and the signal amplitude symmetry test.

- Differential output voltage: The +/- Vout differential output voltage tests are used to verify whether the differential output voltage of the device under test(DUT) are within the compliance limits by measuring the average amplitude of the positive and negative pulses of the UTP AOI output waveforms. The voltage amplitude threshold of the standard definition is between +/- (950mV to 1050mV).
- Signal Amplitude Symmetry: Calculates the ratio of the average positive and negative amplitude of the device under test (DUT), with the standard allowable ration range is between 0.98 and 1.02 in the absolute value.

6.2.1 Test procedure

1) Select **Peak Voltage (ANSI X3.263-1995,9.1.2.2 and 9.1.4)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /idle/ code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel and pulse width in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test**.
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT “Source” channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test result.
8) The test of signal amplitude symmetry requires the results of differential output voltages (positive pulse width and negative pulse width), so it will be automatically test differential output voltages before performing the signal amplitude symmetry test.

6.2.2 Algorithm

For the peak voltage test item, in section 9.1.2.2 of ANSI X3.263-1995 standard, which defines the test signal: an output waveform consisting of 14 bit times (112ns pulse width) of no transition preceded by a transition from 0 V to Vout. The reference waveform in the standard definition assumes that the DUT sends scrambled, MLT-3 encoded/H/code-group, but this type of signal is much easier to obtain for FDDI devices. However, it is difficult to let 100 BASE-TX devices to generate 14bit (112ns) of no transition waveforms. Usually, the device under test (DUT) will be allowed to send out MLT-3 idle waveforms, from which 12bit (96ns) of no transition waveforms will be obtained to replace the

waveforms with 14bit (112ns) pulse width. Siglent's Ethernet Compliance Software supports acquiring waveforms with 80ns and 96ns pulse widths.

The differential output voltage (positive pulse width) is measured when the +Vout signal shifts from 0V to +Vout, this time range extends from 8 ns after the signal rise crosses 50% of +Vout to 8 ns before the signal fall crosses 50% of +Vout, calculate the mean voltage over this range, and the test waveforms are shown in Figure 6-4.

The measurement algorithm for differential output voltage (negative pulse width) is similar to the measurement for differential output voltage (positive pulse width).

The absolute value of both the +/- Vout amplitude of the transmitter differential output voltage should between 950 mV and 1050 mV.

The signal amplitude symmetry is computed as follows:

Symmetry = | +Vout/ -Vout |

The allowable range is 0.98 to 1.020.

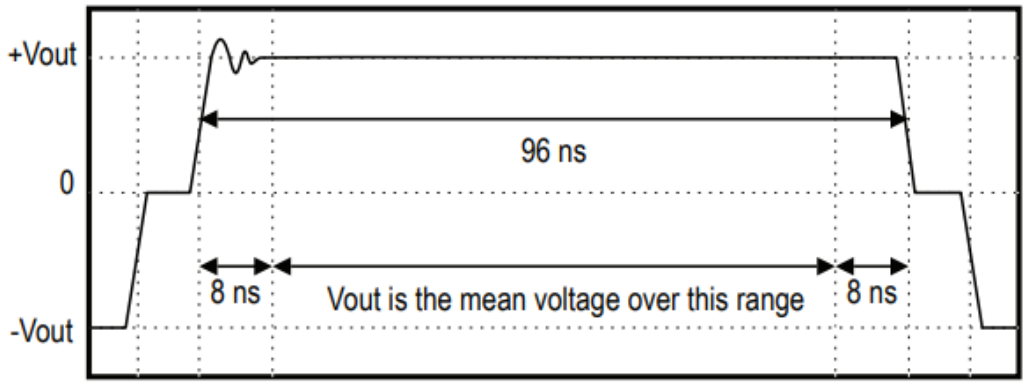

Figure 6-4 Peak Voltage Test Waveform Example

6.2.3 Test Results Reference

The test results are shown in Figure 6-5 and Figure 6-6.

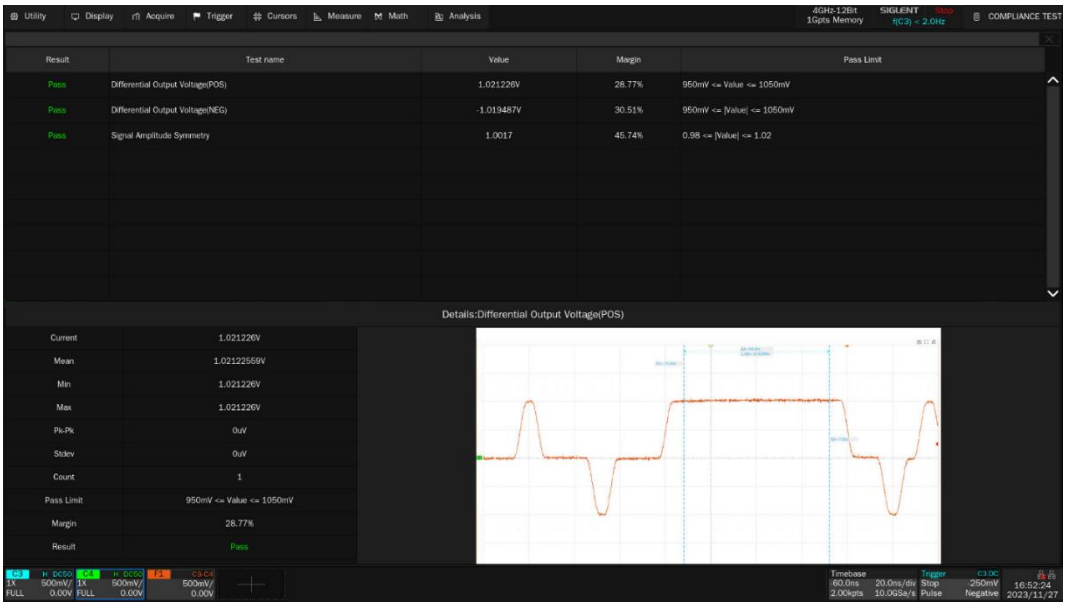

Figure 6-5 Peak Voltage Test Results

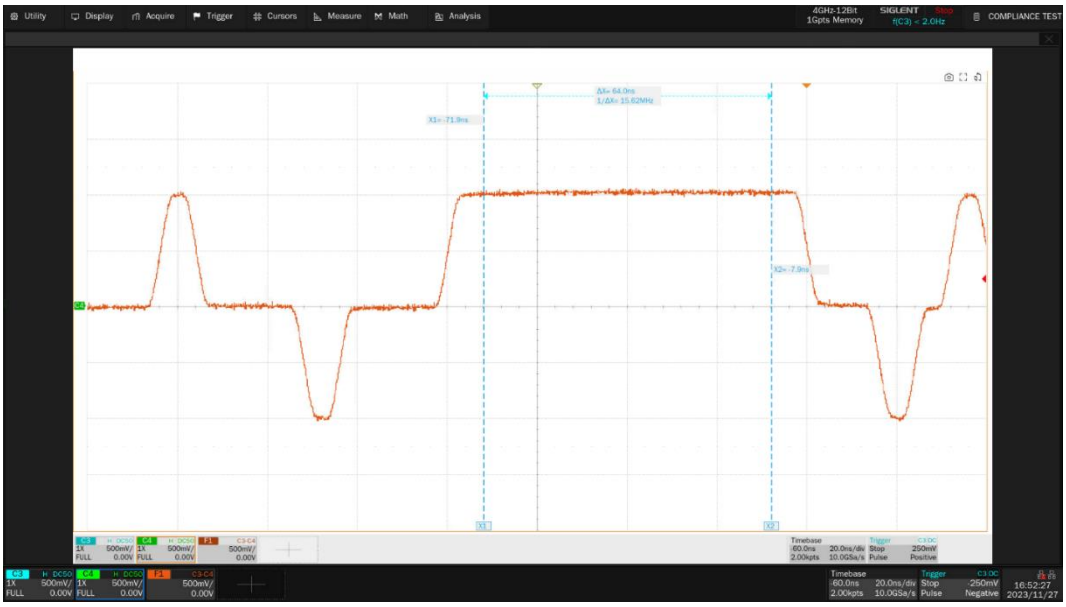

Figure 6-6 Details for Peak Voltage Test Waveform

6.3 Overshoot Tests

The UTP +/-Vout Differential Output Voltage tests are to verify that the waveform overshoot of the device under test (DUT) is within the conformance limits.

6.3.1 Test procedure

1) Select **Overshoot (ANSI X3.263-1995,9.1.3)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /idle/ code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel and pulse width in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test** .
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT “Source” channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test result.

6.3.2 Algorithm

In this test, the specification does not define a reference waveform, the same waveform as the peak voltage test is used for this test item, which is shown as in Figure 6-4.

Waveform overshoot is defined as the relative percentage of the worst excursion of the signal transition beyond its final adjusted value. Accurately determining the end of the signal transition may be difficult.

The waveform overshoot is determined as follows:

1) Measure the peak voltage over the waveform from the time of the 50% crossing point to a time 8 ns after this point. Define this worst excursion as Vpeak.
2) Measure the stable output voltage Vout.
3) Calculate the waveform overshoot by using (Vpeak-Vout)/Vout*100%.

The reference waveform for overshoot test is shown in Figure 6-7.

The waveform overshoot must be less than 5%. Waveform overshoot is computed using the above method for both positive going and negative going transitions. In compliance mode, averaging is used to reduce measurement noise and increase measurement resolution.

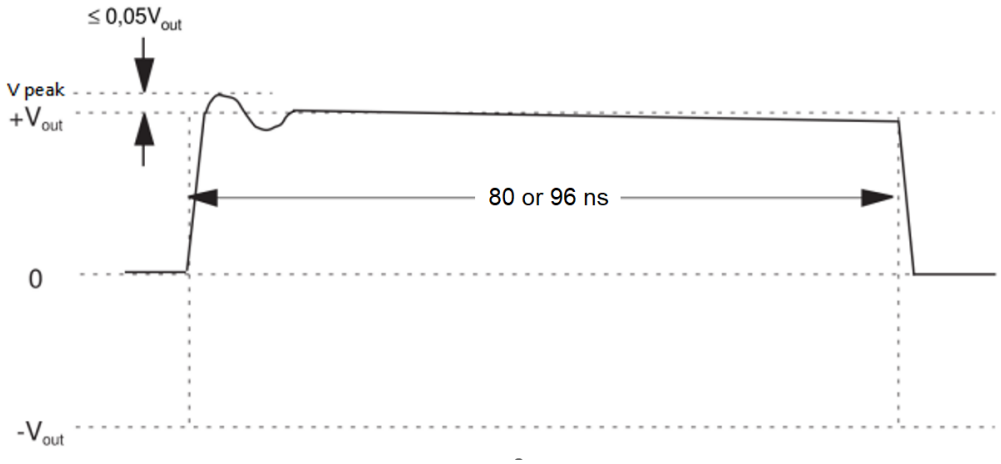

Figure 6-7 Waveform Overshoot Reference Waveform

6.3.3 Test Results Reference

The overshoot (rise edge and fall edges of the pulse) of the transmitter output signal must not exceed 5%.

The overshoot test result reference is shown in Figure 6-8 and the waveform details is shown in Figure 6-9.

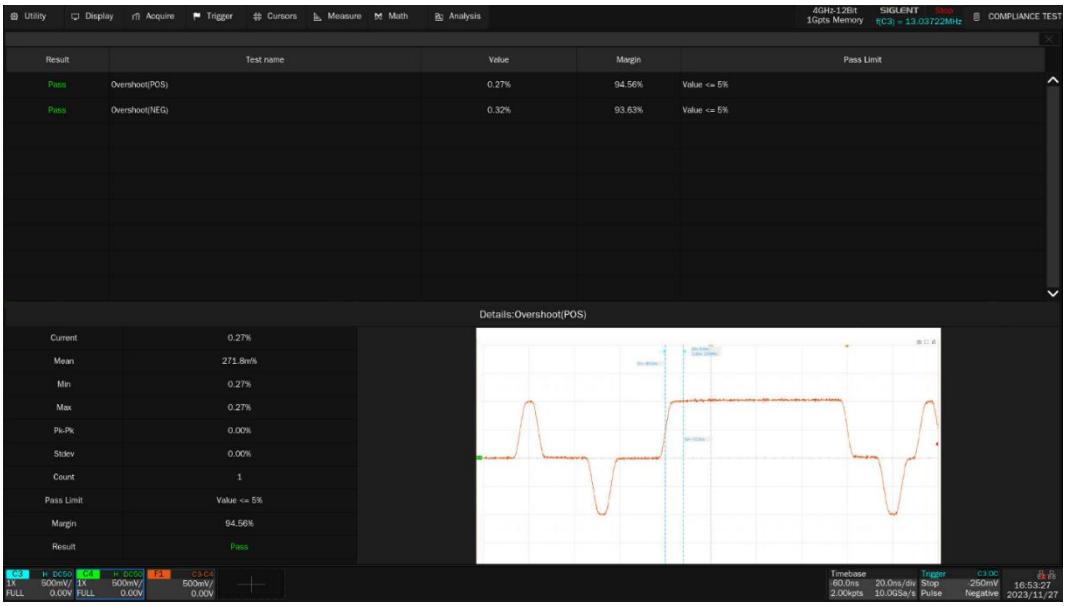

Figure 6-8 Overshoot Test Results

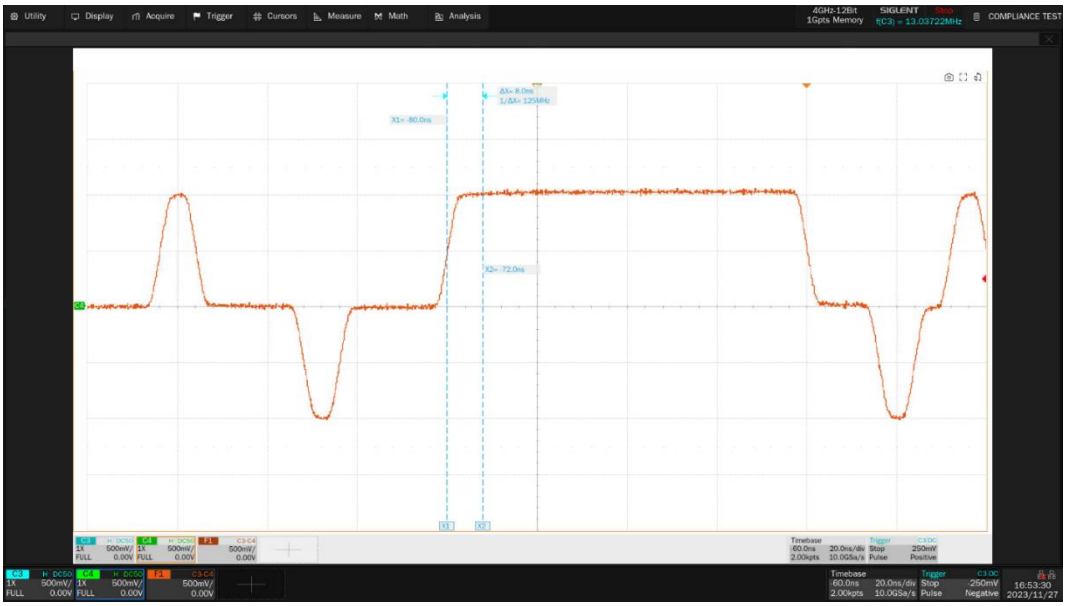

Figure 6-9 Details for Overshoot Test Waveform

6.4 Rise and Fall Time Tests

For the 100 BASE-TX rise and fall time tests, the rise time and fall time measurements for positive and negative pulse widths, as well as symmetry calculations, are included as follows:

- AOI + Vout Rise Time: To verify the DUT's rise time of the positive pulse width (0V to +Vout) is within the compliance limits, which is of 3~5ns.
- AOI + Vout Fall Time: To verify the DUT's fall time of the positive pulse width (+Vout to 0V) is within the compliance limits, which is of 3~5ns.
- AOI + Vout rise/fall time symmetry: The difference between the rise time and fall time of the positive pulse width of the DUT should be within 500ps.
- AOI - Vout Rise Time: To verify the DUT's rise time of the negative pulse width (0V to -Vout) is within the compliance limits, which is of 3~5ns.
- AOI - Vout Fall Time: To verify the DUT's fall time of the negative pulse width (-Vout to 0V) is within the compliance limits, which is of 3~5ns.
- AOI - Vout rise/fall time symmetry: The difference between the rise time and fall time of the negative pulse width of the DUT should be within 500ps.
- AOI overall rise/fall time symmetry: the difference between the maximum rise time or fall time and the minimum rise time or fall time in positive and negative pulse of the DUT should be within the conformance limits, which is 500ps.

6.4.1 Test procedure

1) Select **Rise/Fall Times(ANSI X3.263-1995,9.1.6)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /idle/ code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel and pulse width in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test** .
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT "Source" channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test result.
8) The calculation of rise and fall time symmetry is based on rise and fall time test result, so rise and fall time tests must be done before rise and fall time symmetry tests.

6.4.2 Algorithm

According to the section 9.1.6 of ANSI X3.263-1995 standard, the rise time and fall time of the transmitter output signals (10% to 90%, positive edge and negative edge) should all be within the conformance limits(3ns to 5ns), and the distribution of all measured results of rise and fall time should be less than 0.5 ns.

6.4.3 Test Results Reference

The list of rise and fall time test results is shown in Figure 6-10, and details of one test waveform of the rise time is shown in Figure 6-11.

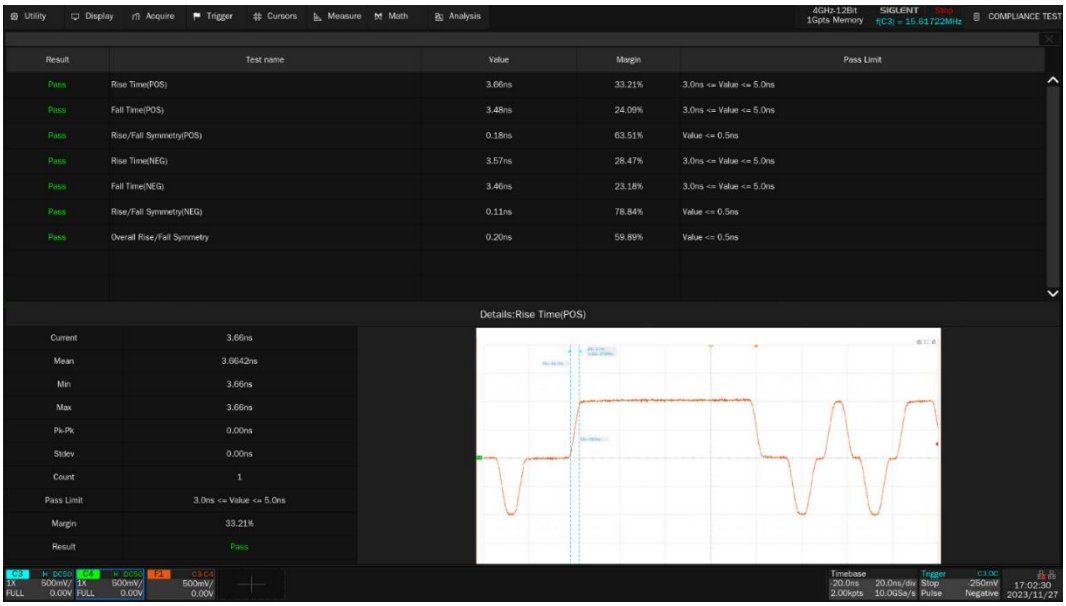

Figure 6-10 Rise and Fall Time Test Results List

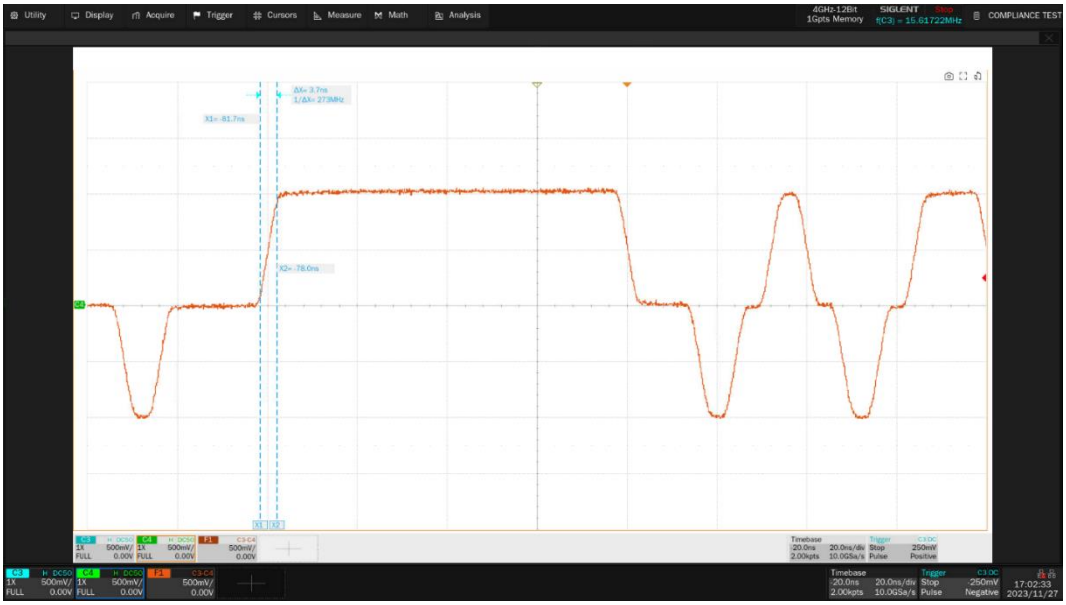

Figure 6-11 Details for Rise Time Test Waveform

6.5 Duty Cycle Distortion Tests

The 100 BASE-TX duty cycle distortion test requires that the peak-to-peak duty cycle distortion of the transmitter's output signal should be within the compliance limits.

6.5.1 Test procedure

1) Select **Duty Cycle Distortion (ANSI X3.263-1995,9.1.8)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /idle/ code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test** .
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT "Source" channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test result.

6.5.2 Algorithm

The peak-to-peak duty cycle distortion test is based on the limits of section 9.1.8 of the ANSI X3.263-1995 standard. The test measures the time when the averaged waveform crosses ±Vout/2 volts, which is shown as Figure 6-12.

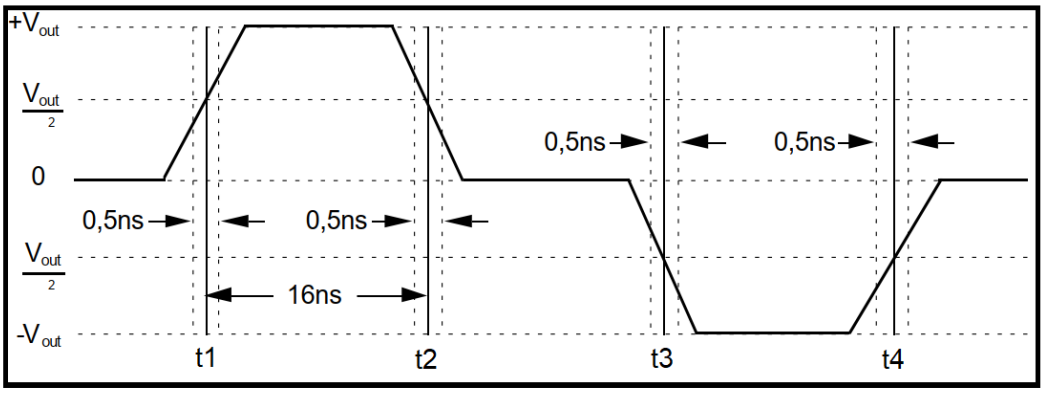

Figure 6-12 Duty Cycle Distortion Test

The software calculate the peak-to-peak duty cycle distortion according to the following formulas:

- T1 = t2 – t1 - 16ns
- T2 = t3 – t2 - 16ns

- T3 = t4 – t3 - 16ns
- T4 = t3 –t1 - 32ns
- T5 = t4 –t2 - 32ns
- T6 = t4 – t1 - 48ns

Peak-to-peak duty cycle distortion equals to the absolute value of maximum (T1, T2, T3, T4, T5, T6). The standard requires maximum peak-to-peak duty cycle distortion should be less than 500ps.

6.5.3 Test Results Reference

The peak-to-peak duty cycle distortion test requires a measurement of the time when the averaged waveform crosses Vout/2 volts, and the test results are shown in Figure 6-13 and Figure 6-14.

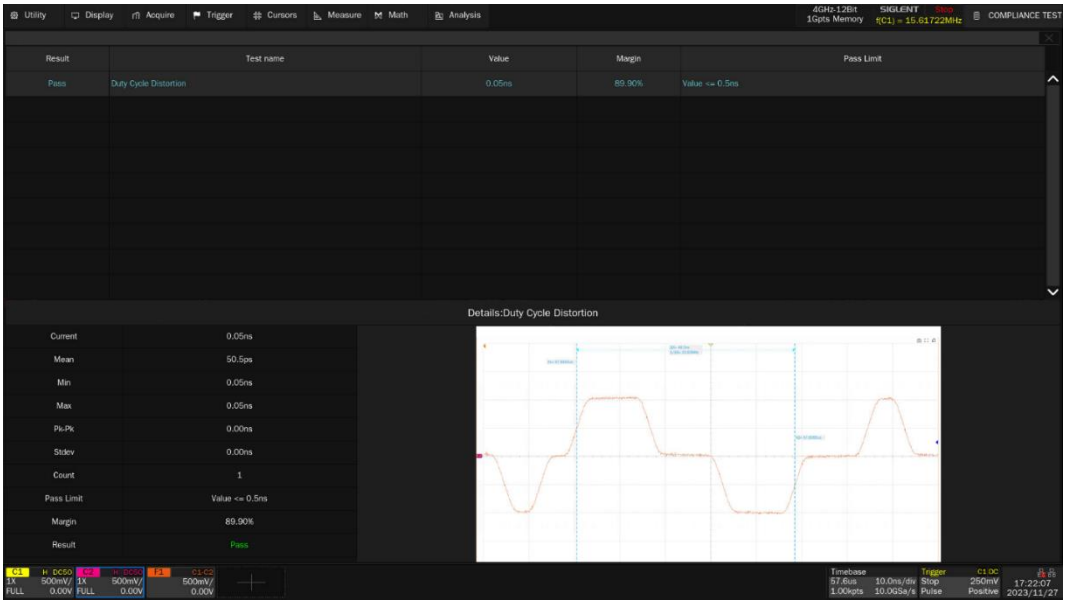

Figure 6-13 Duty Cycle Distortion Test Results

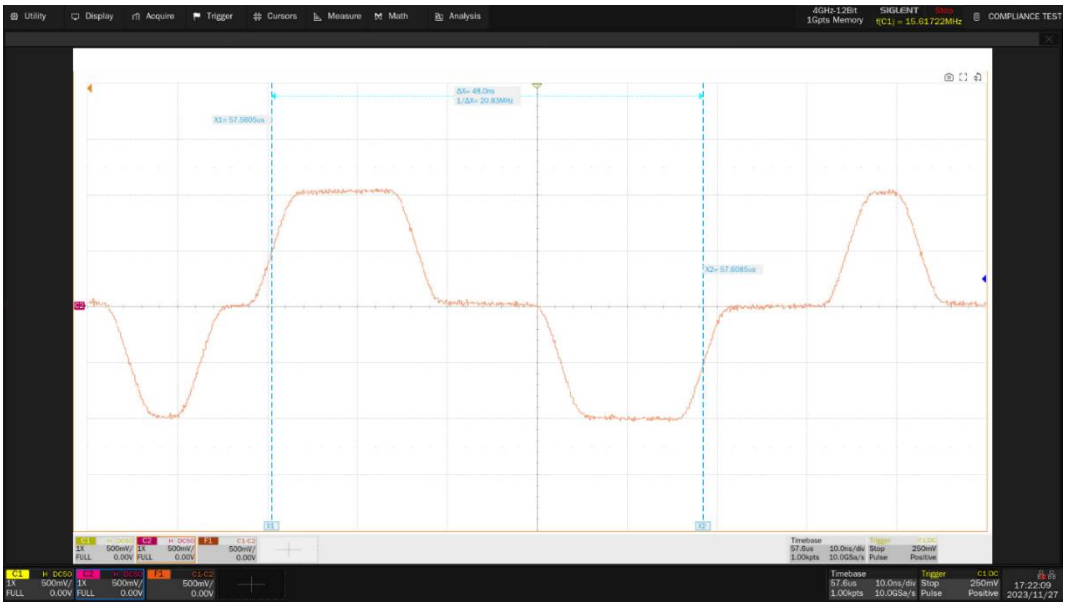

Figure 6-14 Details for Duty Cycle Distortion Test Waveform

6.6 Jitter Tests

The 100 BASE-TX Transmit Jitter test ensures that the total transmit jitter of the signal at the Active Output Interface (AOI) is within conformance limits, which is specified in section 9.1.9 of ANSI X3.263-1995 standard.

6.6.1 Test procedure

1) Select **Peak to Peak Transmit Jitter (ANSI X3.263-1995,9.1.9)** in **Test Select** label.
2) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded / idle / code-groups (this is a 3-level pseudo-random bit sequence).
3) Set the probe type (differential probe or single-ended input), input channel in the **Configure** label.
4) Check the correctness of the test environment setup in the **Connect** label.
5) Click **Run Test** .
6) If the connection is not properly to perform the test, the application will return to the connection step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
7) During the test, the oscilloscope will automatically verify the correct test signal is present on the configured DUT “Source” channel and configure the correct trigger level to capture the signal. After finishing all the tests will output the test result.

6.6.2 Algorithm

For peak-to-peak transmit jitter measurements, the specification does not require the total number of edges or UIs to calculate jitter. Since jitter is a statistical phenomenon with some random component, measuring jitter over a larger population will provide increasingly larger peak-to-peak values (the tails of a Gaussian distribution are infinitely long)

Jitter is the difference between the measured timing instant and the ideal timing reference. The IEEE802.3 standard does not specify whether to use the transmit clock or the recovery clock to be used as the timing reference. To facilitate the test setup, we assume that the recovery clock is used as the timing reference for jitter. The recovery clock is derived from the data signal by applying the software equivalent of a 125 MHz phase-locked loop (PLL). The 125 MHz phase-locked loop (PLL) is phase-locked to the data signal.

For peak-to-peak jitter value in compliance limits, the standard requires the value less than 1.4ns.

6.6.3 Test results reference

The test results of peak-to-peak jitter are shown in Figure 6-15 and Figure 6-16.

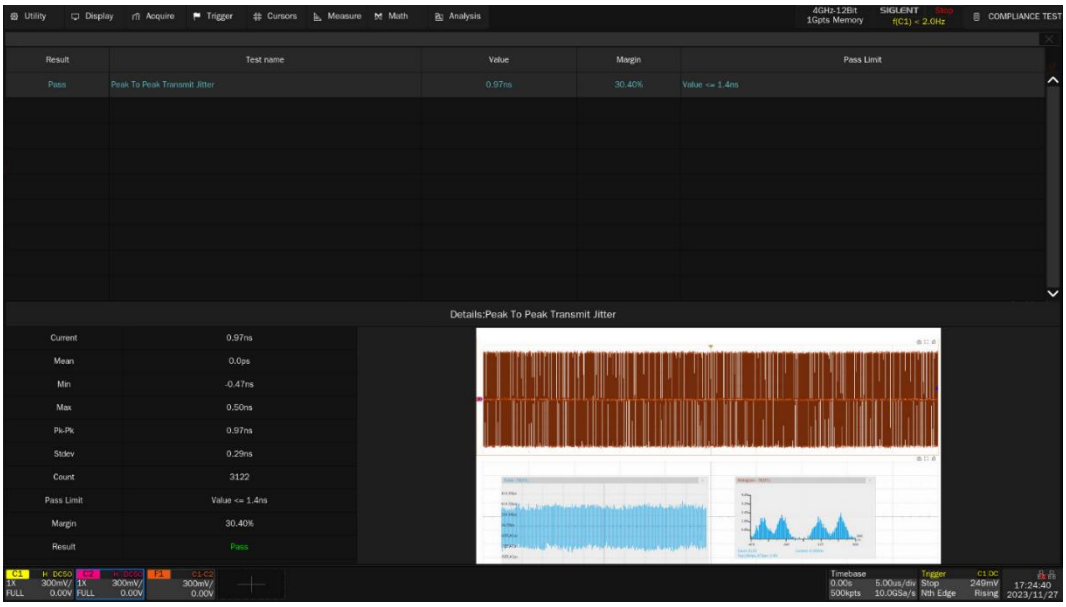

Figure 6-15 Peak-to-Peak Jitter Test Results

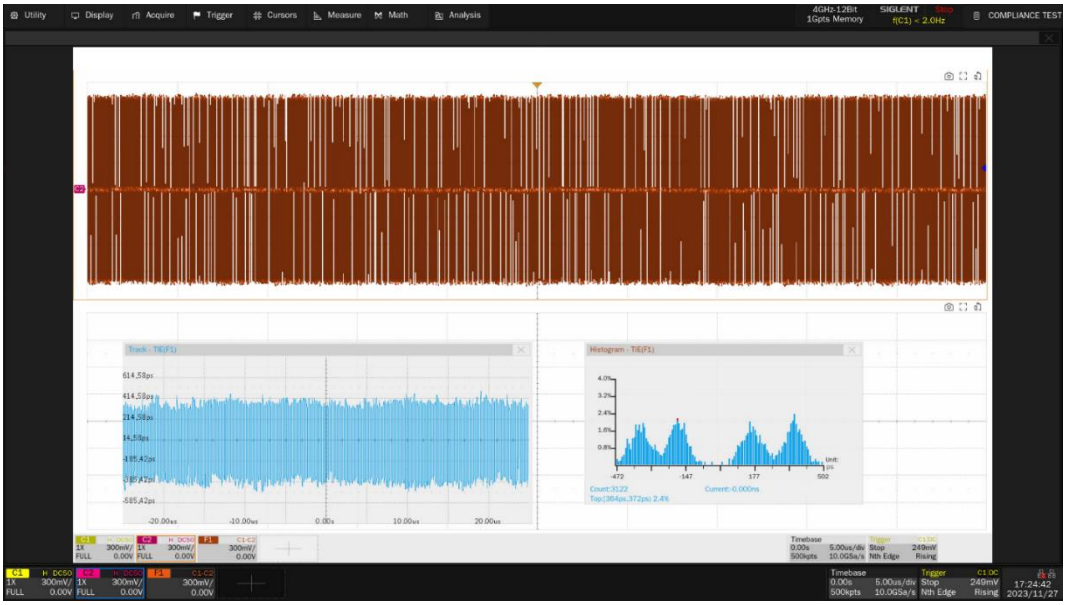

Figure 6-16 Details for Peak-to-Peak Jitter Test Waveform

6.7 Transmitter Return Loss Tests

MDI return loss tests for 100 BASE-TX transmitter is performed according to Subclause 9.1.5 of ANSI X3.263-1995, which describes the 100 BASE-TX transmitter return loss test specification. A VNA is required to perform the return loss test, which involves the steps for VNA calibration before testing return loss.

6.7.1 VNA Calibration Procedure

For the transmitter return loss test, the VNA needs to calibrate before measuring the MDI return loss. The VNA calibration procedure is as follows:

1) On the test fixture, use two SMA cables with equal length to connect the J47 and J52 connectors on section ② to J17(DA-) and J4(DA+) connectors on section ⑥.
2) Use a SMA cable to connect one port on VNA to J48 connector on Section ② of the test fixture.
3) Connect the other unused test points on section ⑥ of the test fixture with 50Ω terminators.
4) Use a Type A-Type B USB cable to connect the USB Host port on the oscilloscope to the USB Device port on the VNA.
5) On the test fixture, use a short UTP cable to connect J46 connector on section ⓪ to J27 connector on section ⑥.
6) On the **Test Select** label, click **Return Loss (ANSI X3.263-1995, 9.15 and 9.2.2)** -> **Transmitter Return Loss** .On the **Configure** label, click **Test Item** -> **Return Loss** -> **Connect Test** , the oscilloscope will detect the VNA connection status, if the VNA is detected, then the VNA's Model Name will appear, and the Oscilloscope will automatically carry out the VNA setting(automatically setting only supports Siglent's VNA).The following is a list of VNA setup:
   - Set the measurement type (Meas) to Return Loss (e.g., S11);
   - Set the start frequency to 2 MHz;
   - Set the stop frequency to 80 MHz;
   - Set the IF bandwidth to 100Hz;
   - Set the number of scan points to 500;
   - Enables continuous scanning;
7) Click **VNA Port Select** to select the VNA port being used, Click **VNA Calibration** -> **Open** to perform Open calibration.
8) For Short and Load calibration, change the short UTP cable connection and then click Short and Load to perform calibration respectively.

The calibration environment for the VNA is shown in Figure 6-17.

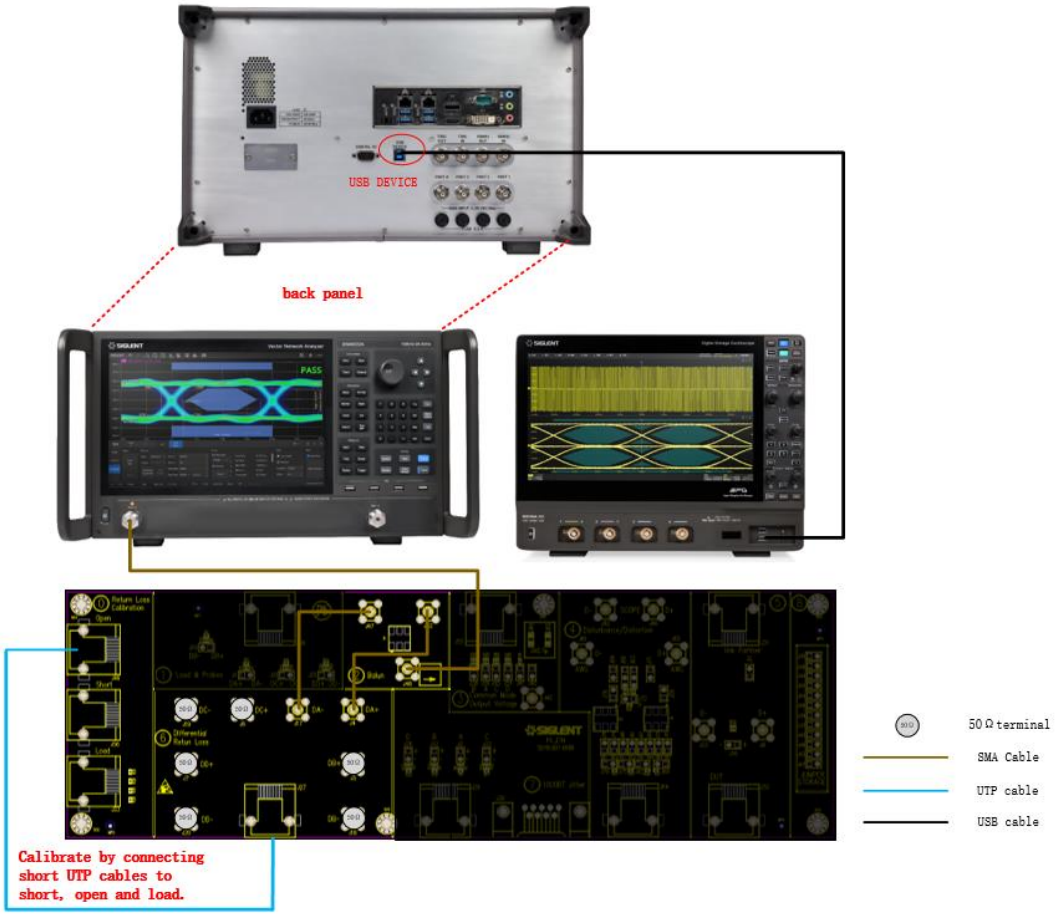

Figure 6-17 VNA Calibration Environment

6.7.2 Test procedure

The test procedure is as follows:

1) Configure the DUT for 100 BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded / idle / code-groups (this is a 3-level pseudo-random bit sequence).
2) On the test fixture, use two SMA cables with equal length to connect the J47 and J52 connectors on section ② to J17(DA-) and J4(DA+) connectors on section ⑥.
3) Use a SMA cable to connect one port on VNA to J48 connector on Section ② of the test fixture.
4) Connect the other unused test points on section ⑥ of the test fixture with 50Ω terminators.
5) Use a Type A-Type B USB cable to connect the USB Host port on the oscilloscope to the USB Device port on the VNA.
6) On the Oscilloscope, Click **Run Test** , and click **Run Test** when the pop-up window appears, and the Oscilloscope will automatically acquire the return loss data tested by the VNA, and plots the curve, and output the test result.

The connection is shown as Figure 6-18.

Figure 6-18 Transmitter Return Loss Test Environment

6.7.3 Algorithm

Subclause 9.1.5 of ANSI X3.263-1995 standard describes return loss specifications for 100 BASE-TX devices physical medium attachment (PMA). The UTP and STP AOI interface shall be implemented such that the following return loss characteristics are satisfied for each of the specified line impedances:

- Less than -16dB from 2MHz to 30MHz;
- Less than -(16-20log10(f/30 MHz)) dB from 30 MHz to 60 MHz;
- Less than -10dB from 60MHz to 80MHz.

The impedance for measuring the return loss of the UTP AOI is 100 Ω ± 15 Ω. The impedance environment should be resistive, and the magnitude of the phase angle should be less than 3° over the specified measurement frequency range. The software will convert the return loss data from 100Ω to 85Ω and 115Ω to determine whether it is within the threshold range.

6.7.4 Test results reference

The transmitter return loss tests are shown in Figure 6-19 and Figure 6-20.

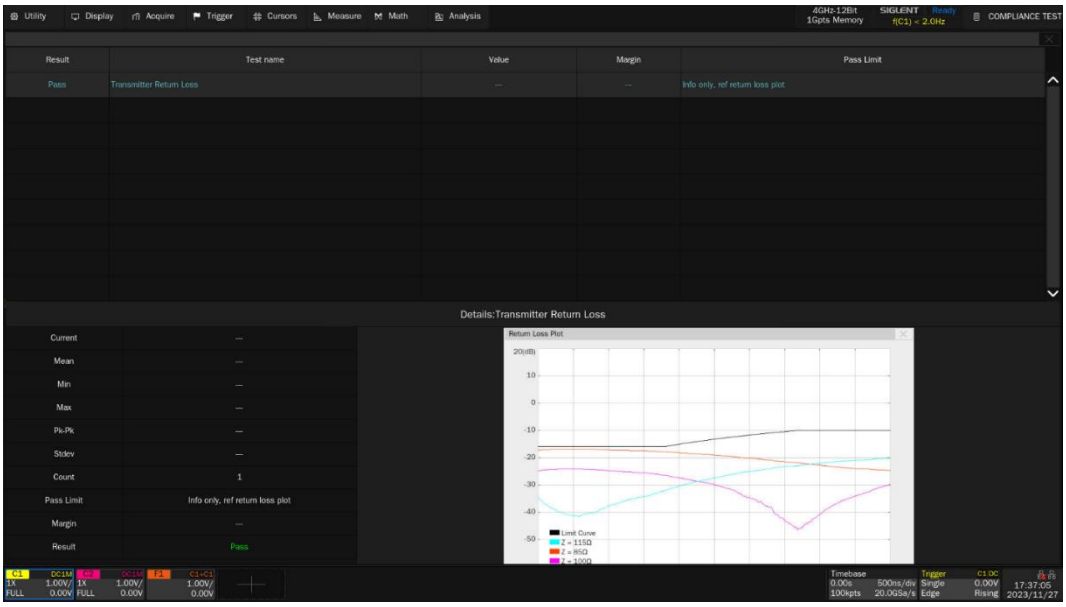

Figure 6-19 Transmitter Return Loss Test Results

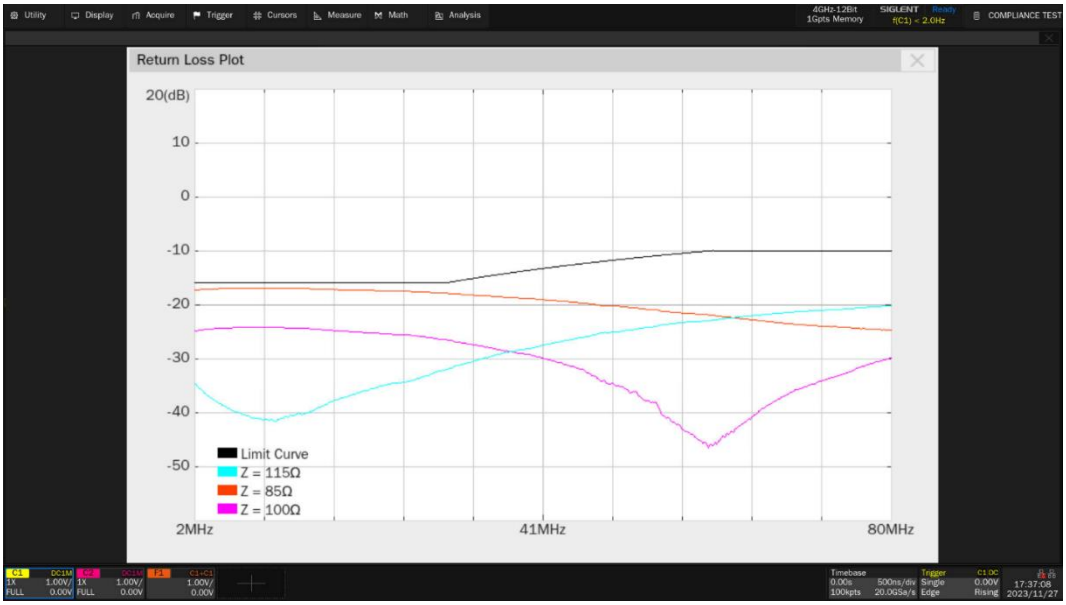

Figure 6-20 Details for Transmitter Return Loss Waveform

6.8 Receiver Return Loss Tests

This section describes the 100 BASE-TX Receiver Return Loss test according to ANSI X3.263-1995, Subclause 9.2.2. The test procedures described in this section cover the Receiver Return Loss measurement required by the specification.

6.8.1 VNA Calibration Procedure

For the receiver return loss test, the VNA needs to calibrate before measuring the MDI return loss. The VNA calibration procedure is as follows:

1) On the test fixture, use two SMA cables with equal length to connect the J47 and J52 connectors on section ② to J18(DB-) and J5(DB+) connectors on section ⑥.
2) Use a SMA cable to connect one port on VNA to J48 connector on Section ② of the test fixture.
3) Connect the other unused test points on section ⑥ of the test fixture with 50Ω terminators.
4) Use a Type A-Type B USB cable to connect the USB Host port on the oscilloscope to the USB Device port on the VNA.
5) On the test fixture, use a short UTP cable to connect J46 connector on section ⓪ to J27 connector on section ⑥.
6) On the **Test Select** label, click **Return Loss (ANSI X3.263-1995, 9.15 and 9.2.2)** -> **Receiver Return Loss** .On the **Configure** label, click **Test Item** -> **Return Loss** -> **Connect Test** , the oscilloscope will detect the VNA connection status, if the VNA is detected, then the VNA's Model Name will appear, and the Oscilloscope will automatically carry out the VNA setting(automatically setting only supports Siglent's VNA).The following is a list of VNA setup:
   - Set the measurement type (Meas) to Return Loss (e.g., S11);
   - Set the start frequency to 2 MHz;
   - Set the stop frequency to 80 MHz;
   - Set the IF bandwidth to 100Hz;
   - Set the number of scan points to 500;
   - Enables continuous scanning;
7) Click **VNA Port Select** to select the VNA port being used, Click **VNA Calibration** -> **Open** to perform Open calibration.
8) For Short and Load calibration, change the short UTP cable connection and then click Short and Load to perform calibration respectively.

The calibration environment for the VNA is shown as Figure 6-21.

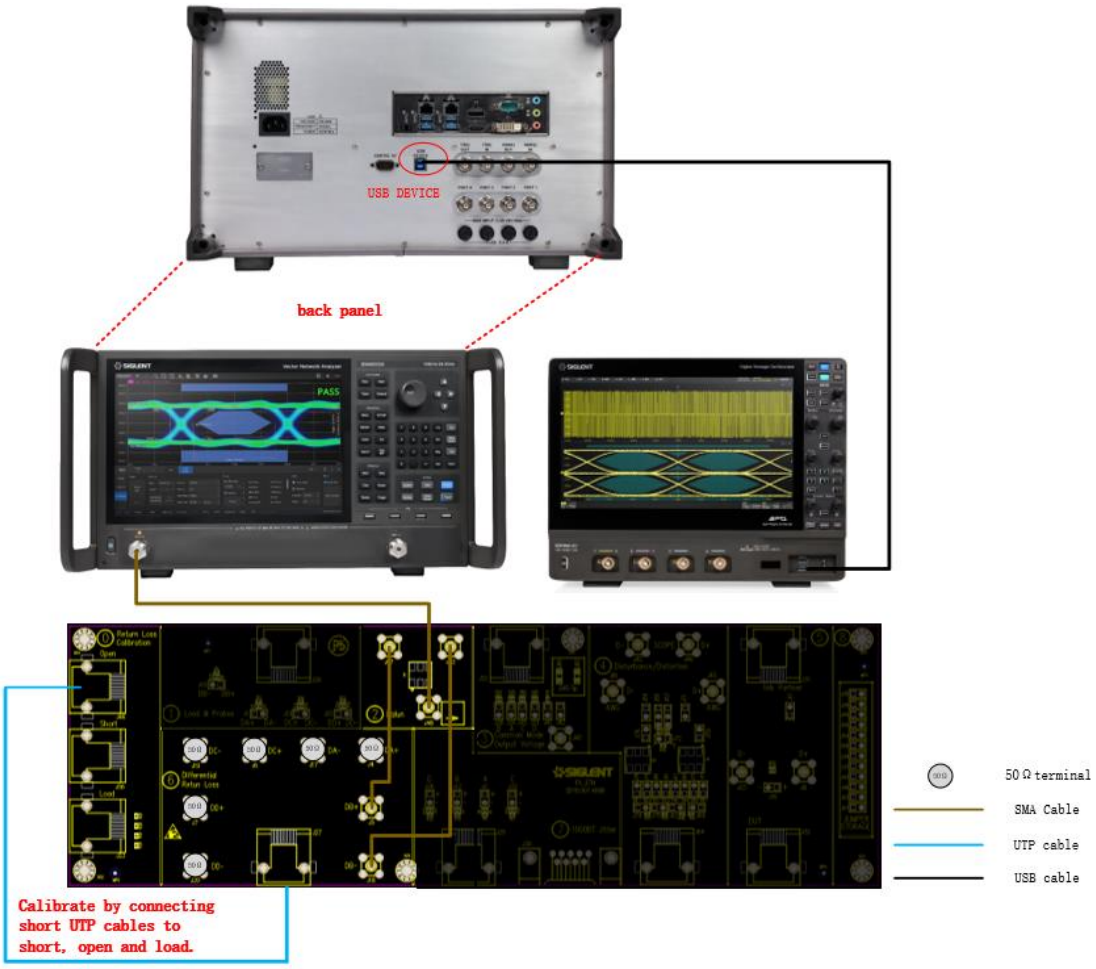

Figure 6-21 VNA Calibration Environment for Receiver

6.8.2 Test Procedure

The test procedure for receiver is as follows:

1) The DUT for 100 BASE-TX operation does not require any particular configuration. Simply turn on the DUT and set the DUT to operate in 100 BASE-TX to perform the test.
2) On the test fixture, use two SMA cables with equal length to connect the J47 and J52 connectors on section ② to J18(DB-) and J5(DB+) connectors on section ⑥.
3) Use a SMA cable to connect one port on VNA to J48 connector on Section ② of the test fixture.
4) Connect the other unused test points on section ⑥ of the test fixture with 50Ω terminators.
5) Use a Type A-Type B USB cable to connect the USB Host port on the oscilloscope to the USB Device port on the VNA.
6) On the Oscilloscope, Click **Run Test** , and click **Run Test** when the pop-up window appears, and the Oscilloscope will automatically acquire the return loss data tested by the VNA, and plots the curve, and output the test result.

The connection for return loss test of the receiver is shown as Figure 6-22.

Figure 6-22 Receiver return loss test connection

6.8.3 Algorithm

ANSI X3.263-1995 in 9.2.2 describes return loss specifications for 100 BASE-TX devices at physical medium attachment (PMA). The receiver channel needs to meet the specifications described as below:

- Less than -16dB from 2MHz to 30MHz;
- Less than -(16-20log$_{10}$(f/30 MHz)) dB from 30 MHz to 60 MHz;
- Less than -10dB from 60MHz to 80MHz.

The impedance for measuring the return loss of the UTP AOI is 100Ω ± 15Ω. The impedance environment should be resistive, and the magnitude of the phase angle should be less than 3° over the specified measurement frequency range. The software will convert the return loss data from 100Ω to 85Ω and 115Ω to determine whether it is within the threshold range.

6.8.4 Test Results Reference

The receiver return loss test results are shown in Figure 6-23 and Figure 6-24.

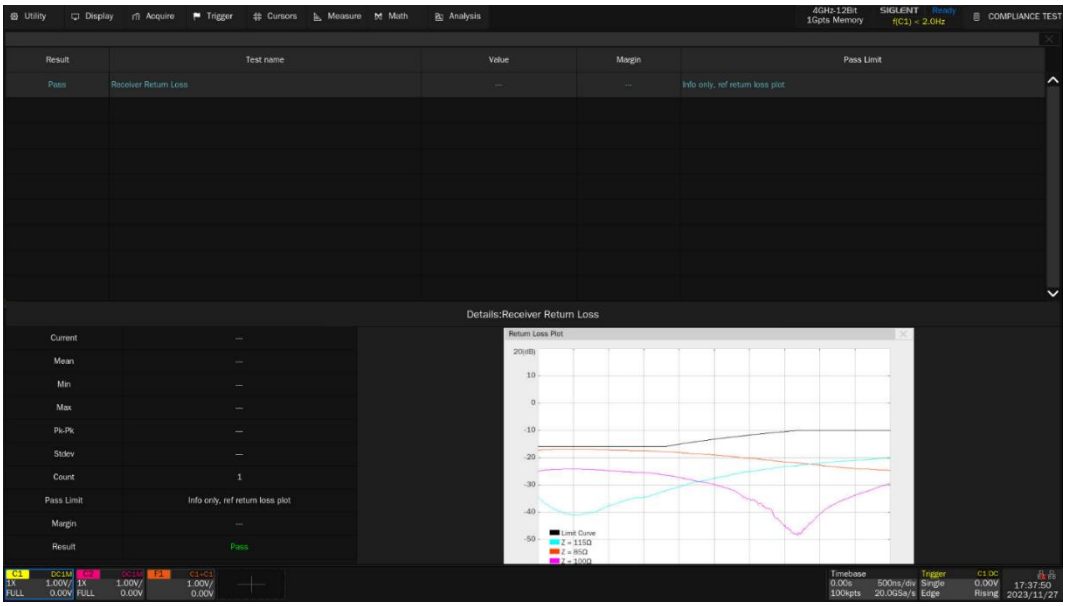

Figure 6-23 Receiver Return Loss Test Results

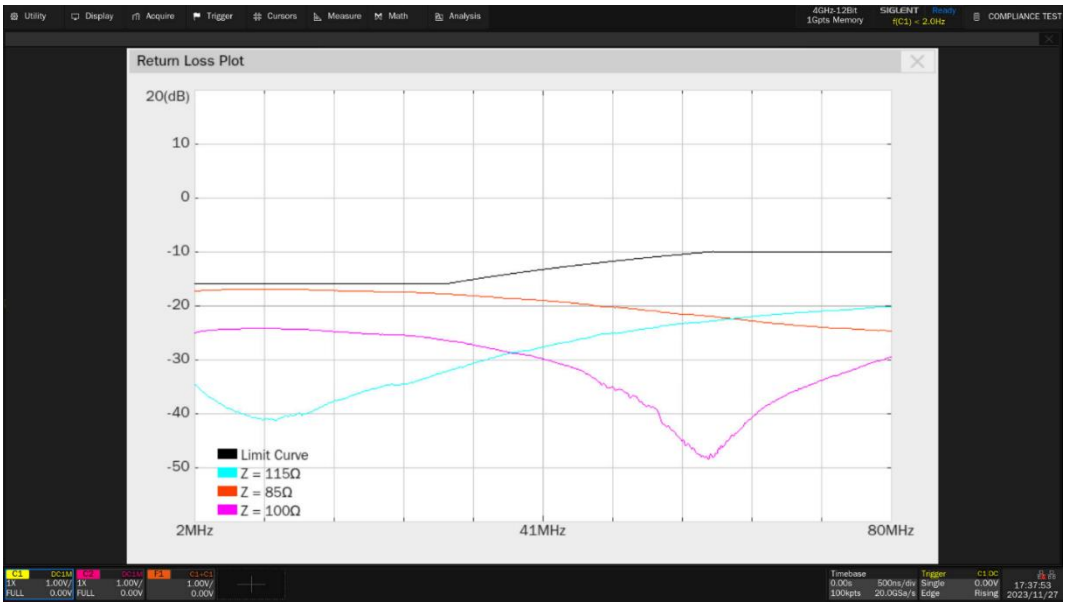

Figure 6-24 Details for Receiver Return Loss Waveform

About SIGLENT

SIGLENT is an international high-tech company, concentrating on R&D, sales, production and services of electronic test & measurement instruments.

SIGLENT first began developing digital oscilloscopes independently in 2002. After more than a decade of continuous development, SIGLENT has extended its product line to include digital oscilloscopes, isolated handheld oscilloscopes, function/arbitrary waveform generators, RF/MW signal generators, spectrum analyzers, vector network analyzers, digital multimeters, DC power supplies, electronic loads and other general purpose test instrumentation. Since its first oscilloscope was launched in 2005, SIGLENT has become the fastest growing manufacturer of digital oscilloscopes. We firmly believe that today SIGLENT is the best value in electronic test & measurement.

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