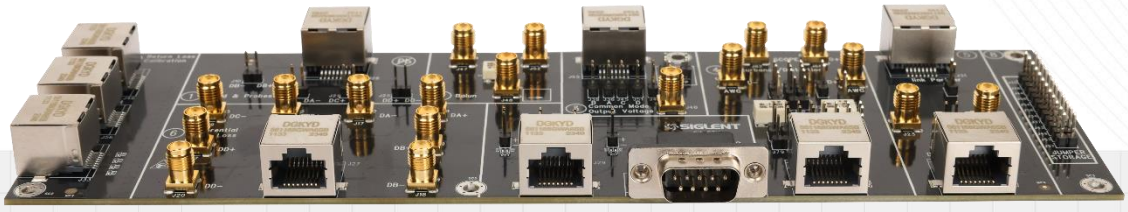
1000 BASE-T Ethernet Compliance Test Application

User Manual

EN01A



SIGLENT TECHNOLOGIES CO.,LTD

Contents

1 Introduction

Siglent provides 100 BASE-TX and 1000 BASE-T Ethernet Compliance Test application to verify the Ethernet transmitter device under test (DUT) compliance to specifications. The equipment required for ethernet conformance tests including Siglent SDS7000A oscilloscope, Vector Network Analyzers, test fixture, probes, Arbitrary Waveform Generator and Ethernet Compliance Test Application software. This user manual only introduces the test fixture, test methods and connection for 1000 BASE-T Ethernet Compliance Test.

The Ethernet Compliance Test Application:

- Let's you select individual or multiple tests to run.
- Shows you how to connect the oscilloscope to the device under test (DUT).
- Automatically sets up the oscilloscope for every test project.
- Provides detailed information for every test that has been run, and lets you know the thresholds at which marginal or critical warnings appear.
- Creates HTML or XML test reports of the tests that have been run.

2 Test Items and Standard Reference

2.1 Test Items

1000 BASE-T Ethernet compliance test is used to verify whether the device under test (DUT) meets the PMA electrical characteristics specified in the IEEE802.3ab standard. It is meaningful to conduct ethernet compliance test during the development process of ethernet devices, which is the guarantee of interoperability performance between devices.

Siglent's compliance test solution for 1000 BASE-T includes the following test items:

- Without Disturber
  - Peak Output Voltage
  - Droop
  - Templates
  - Transmitter Distortion (with TX_TCLK)
  - Transmitter Distortion (Without TX_TCLK)
- With Disturber
  - Peak Output Voltage
  - Droop
  - Templates
  - Transmitter Distortion (with TX_TCLK)
  - Transmitter Distortion (Without TX_TCLK)
- Jitter Without TX_TCLK
  - Jitter Master Mode Filtered
  - Jitter Master Mode Unfiltered
  - Jitter Slave Mode Filtered
  - Jitter Slave Mode Unfiltered
- Jitter with TX_TCLK
  - Jitter Master Mode JTXOUT
  - Jitter Master Mode Filtered
  - Jitter Master Mode Unfiltered
  - Jitter Slave Mode JTXOUT
  - Jitter Slave Mode Filtered
  - Jitter Slave Mode Unfiltered
- Common
  - MDI Return Loss
  - MDI Common-mode Output Voltage

The IEEE802.3ab specification has clear requirements for every test waveform for the compliance test. The DUT is required to provide corresponding waveforms for compliance test according to the

test items. The user can use a software tool that configure the device under test to send out specific test packets according to the requirements.

For all kinds of mainstream NIC chips, you can control the DUT to send out corresponding test waveforms for compliance test by modifying relevant registers or using the packet sending tool provided by the chip manufacturer. IEEE 802.3ab stipulates that setting the 1000 BASE-T chip registers can let the DUT to enter four different test modes, which corresponds to different compliance test items, as Figure 2-1 shown.

The correspondence between test patterns and test items are as follows:

- Test Mode 1: Peak Output Voltage, Droop, Templates.
- Test Mode 2: Transmit jitter test in Master mode.
- Test Mode 3: Transmit jitter test in Slave mode.
- Test Mode 4: Transmitter Distortion, MDI Return Loss, Common-mode Output Voltage.

Table 40–7—GMII management register settings for test modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit waveform test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmitter distortion test
1	0	1	Reserved, operations not identified.
1	1	0	Reserved, operations not identified.
1	1	1	Reserved, operations not identified.

Figure 2-1 1000 BASE-T Test Mode Setting

2.2 Standard Reference

The 1000 BASE-T Ethernet Compliance Test solution from Siglent follows the IEEE802.3-2018, Subclause 40 standard, and Table 2-1 shows the standard reference by every test item.

More information for the IEEE802.3 standard, please go to the website: www.ieee802.org.

Table 2-1 1000 BASE-T Tests by Standard Reference

Standard Reference	Test Mode	Test Items
IEEE 802.3-2018, Subclause 40.6.1.2.1	Test Mode 1	Peak Output voltage tests
IEEE 802.3-2018, Subclause 40.6.1.2.3	Test Mode 1	Templates tests
IEEE 802.3-2018, Subclause 40.6.1.2.2	Test Mode 1	Droop tests
IEEE 802.3-2018, Subclause 40.6.1.2.5	Test Mode 2	Jitter Master unfiltered tests
IEEE 802.3-2018, Subclause 40.6.1.2.5	Test Mode 2	Jitter Master filtered tests
IEEE 802.3-2018, Subclause 40.6.1.2.5	Test Mode 3	Jitter slave unfiltered tests
IEEE 802.3-2018, Subclause 40.6.1.2.5	Test Mode 3	Jitter slave filtered tests
IEEE 802.3-2018, Subclause 40.6.1.2.4	Test Mode 4	Transmitter distortion tests
IEEE 802.3-2018, Subclause 40.8.3.3	Test Mode 4	MDI common mode output voltage tests
IEEE 802.3-2018, Subclause 40.8.3.1	Test Mode 4	MDI return loss tests

3 Test equipment

3.1 Required Equipment

The Ethernet electrical compliance test measurements require the following equipment:

- Oscilloscope (SDS7000A): Oscilloscope's bandwidth larger than 2GHz, and with the Ethernet Compliance Test Application software that has installed the option key (SDS7000A-CT-100BASE-T option for 100BASE-TX, SDS7000A-CT-1000BASE-T option for 1000BASE-T).
- FX-ETH kit: FX-ETH kit is the Ethernet Electrical Compliance Test Fixture from Siglent that provides the physical connection and test points after the DUT enters into the test modes.
- Differential probe or SMA cables:
  - Differential probe (e.g., SAP2500D or SAP5000D): bandwidth greater than 2 GHz for probing signals;
  - SMA cables: connects from the oscilloscope to the test fixture for probing signals.
- Vector network analyzer: VNA is used for MDI return loss test.
- USB Connection Cable: The cable is used to connect the USB Host port on the oscilloscope to the USB Device port on the vector network analyzer, so that the oscilloscope can control and configure the network analyzer and obtain the return loss test data.
- Arbitrary waveform generator: On the 1000BASE-T compliance tests, when the DUT enters Test Mode 1 or Test Mode 4, for the Peak Output Voltage tests, Templates tests, Droop tests, Transmitter Distortion tests with disturbing signal, a dual-channels arbitrary waveform generator which outputs the required disturbing signals.
- Jitter test cable: On the 1000BASE-T compliance tests, when the DUT enters Slave mode, for the jitter tests with TX_TCLK, a 103m long cable is required to connect the DUT to the Link Partner.

3.2 Delivery Checklist

The FX-ETH kit includes the items listed in Table 3-1. When you receive the FX-ETH kit, firstly, verify that all items listed on the checklist have been received. If you notice any omissions or damage, please contact to your nearest Siglent customer service center or distributor as soon as possible. If you fail to contact us immediately in case of omissions or damage, we will not be responsible for replacement.

Table 3-1 FX-ETH Kit Checklist

Item name	Quantities
User Manual	1
Test Fixture Board	1
UTP RJ45 Cable（6 inches）	1
50Ω Terminators（SMA）	8

SMA cables	4
BNC-to-SMA Adaptors	4
Jumpers	12

3.3 Introduction to FX-ETH Test Fixture

FX-ETH kit is the Ethernet Electrical Compliance Test Fixture which cooperates with software for 100 BASE-TX and 1000 BASE-T ethernet compliance validation on SDS7000A.

The test fixture board shown in Figure 3-1 which consists of 9 sections, every section has some specific functions, which are clearly marked on the board to help user to use the test fixture.

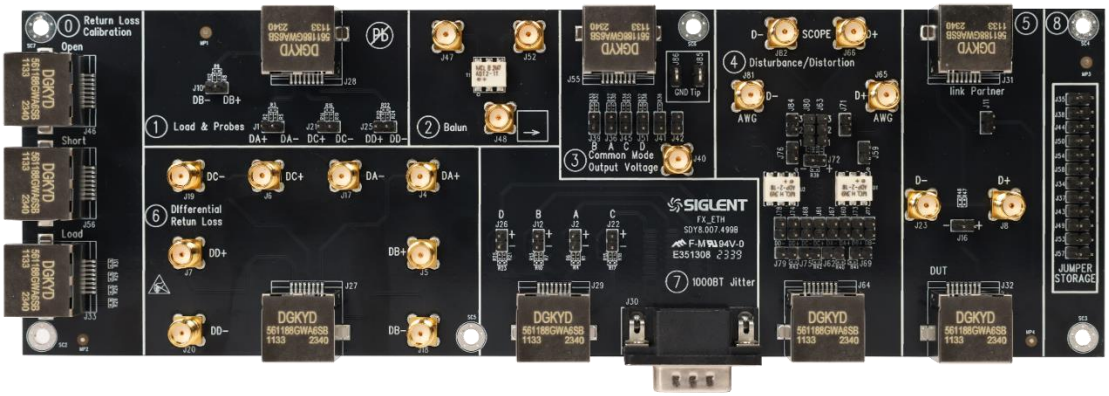


Figure 3-1 Ethernet Electrical Compliance Test Fixture Board

Every section on the board is described as follows:

Section 0: Return loss calibration section. The vector network analyzer can be calibrated for Open, Short, and Load when DUT runs return loss tests.

Section 1: Supports most of the compliance tests for 100 BASE-TX and 1000 BASE-T by using a differential probe.

Section 2: Differential to single-ended signal conversion by using a balun, which supports return loss tests by using one Port on the VNA.

Section 3: Supports for 1000 BASE-T MDI common-mode output voltage tests.

Section 4: Supports Test Mode 1 and Test Mode 4 on 1000Base-T compliance tests with disturbing signals.

Section 5: Under 100 BASE-TX compliance tests, the Link Partner such as the SDS7000A oscilloscope transmits at 100Mbps. The DUT transmitter should then emit the following waveform to support the compliance tests.

Section 6: Supports most of the compliance tests for 100 BASE-TX and 1000 BASE-T by using two SMA cables.

Section 7: Supports 1000 BASE-T jitter tests.

Section 8: Jumper storage section, which can store 12 jumpers.

4 Compliance Test Software

Siglent's 1000Base-T Ethernet Compliance Test is a solution based on IEEE802.3ab and IEEE802.3-2018, Subclause40 specifications. The Ethernet Compliance Application software controls the oscilloscope to automatically perform the tests. The graphical operation guide simplifies the measurement process, the test items can be flexibly configured, and the test report records the entire measurement results, including the test values and the screenshots of the test waveforms.

SDS7000A provides 1000 BASE-T Compliance Test function, according to **Analysis** -> **Compliance Test** -> **Protocol Type** , select **1000 BASE-T** and click **ON** to activate the compliance test function, which is shown in Figure 4-1. The compliance test function is divided into three main parts: **Test Config** , **Results** , and **Report Setting** .

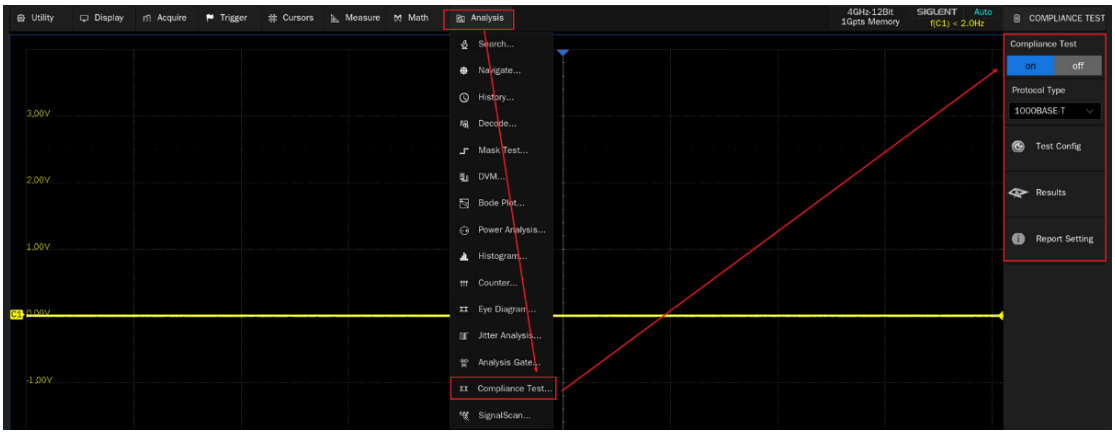


Figure 4-1 Launching 1000 BASE-T Compliance Analysis Software

4.1 Test Configuration

Clicking on **Test Config** will bring up the specific test configuration window, as shown in Figure 4-2, which is divided into six steps based on the test process: **Setup** , **Test Select** , **Configure** , **Connect** , **Run Test** , and **Result** .

- **Setup:** Provide the functions of " **Recall** ", " **Last** " and " **Save** " for the configuration.

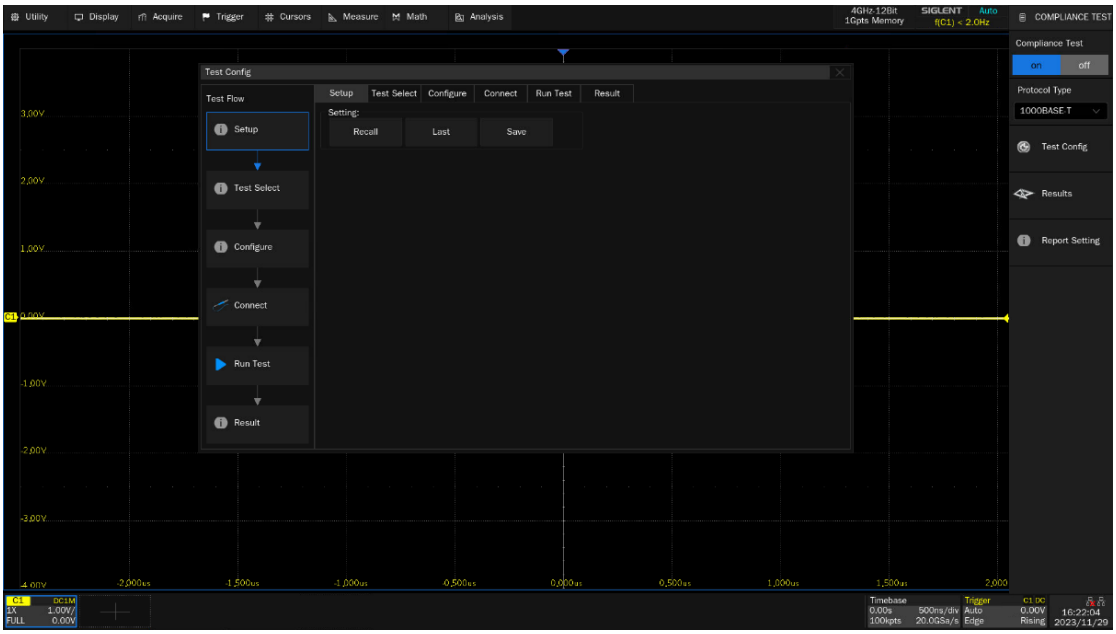


Figure 4-2 Test Configuration window

➢ **Test Select:** Select the items to be tested in this column, as shown in Figure 4-3.

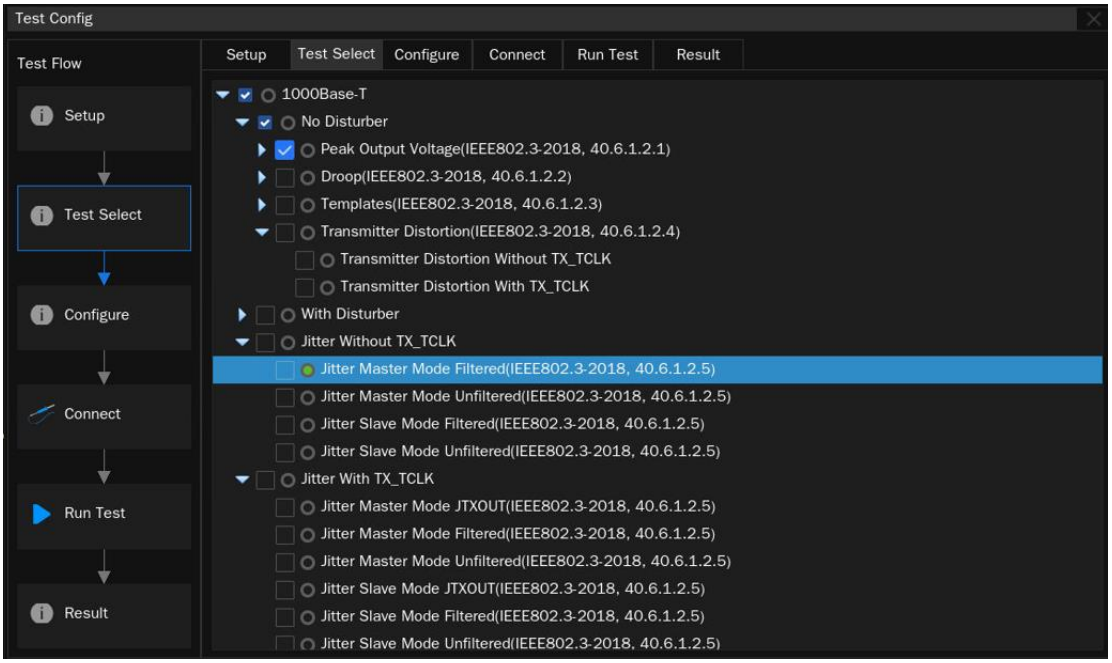


Figure 4-3 Test Items selection window

➢ **Configure:** The test items selected in **Test Select** will be highlighted in this column, and you can click the corresponding items to configure. You can set the input channels and probe types, as shown in Figure 4-4.

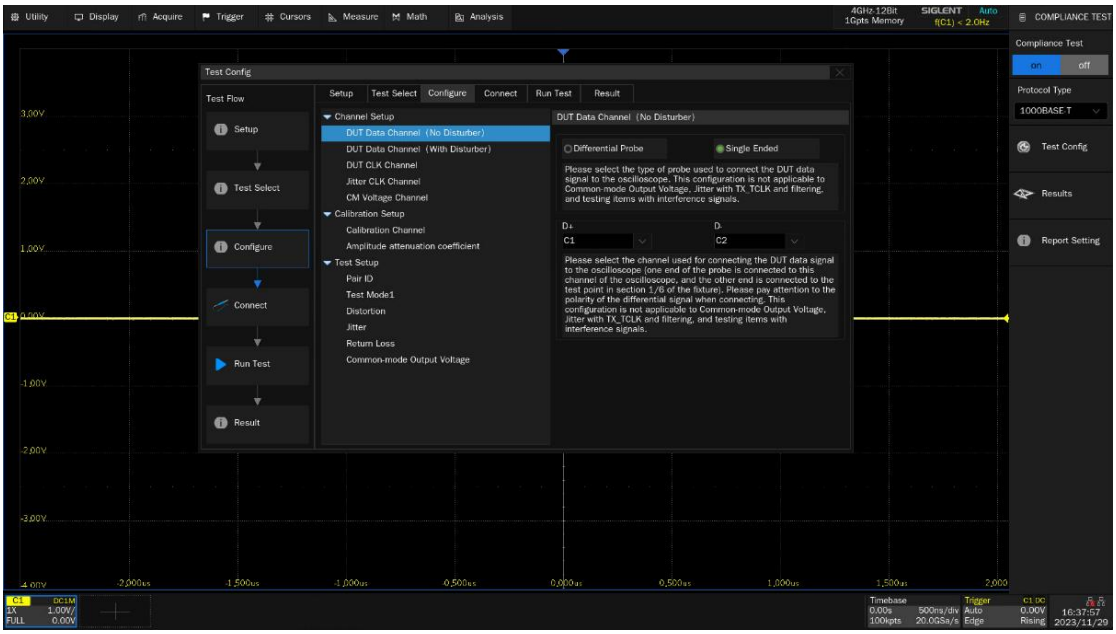


Figure 4-4 Configuration window

- **Connect:** This column displays the connection diagram of the compliance test, as shown in Figure 4-5. If more than one item is selected simultaneous, only the connection diagram for the first test item will be displayed. For the other test items, if the connection is different then a new pop-up window will appear at the end of the previous test.

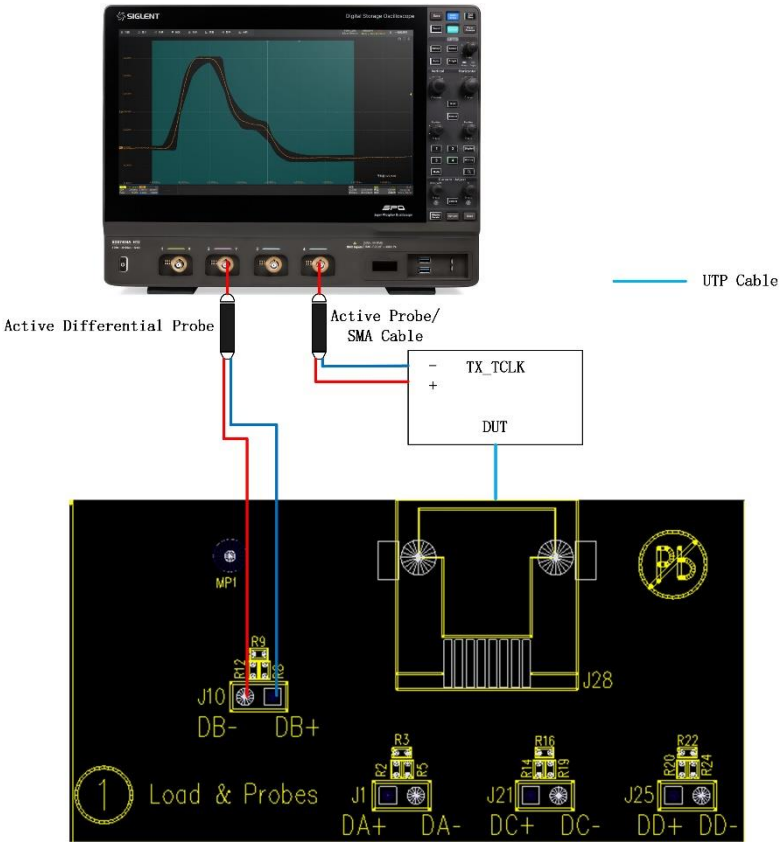


Figure 4-5 Connection diagram in the Connect menu

- **Run Test:** The Run Test window is shown in Figure 4-6. Both " **Continue** " and " **Stop** " options are supported when meets test failures.

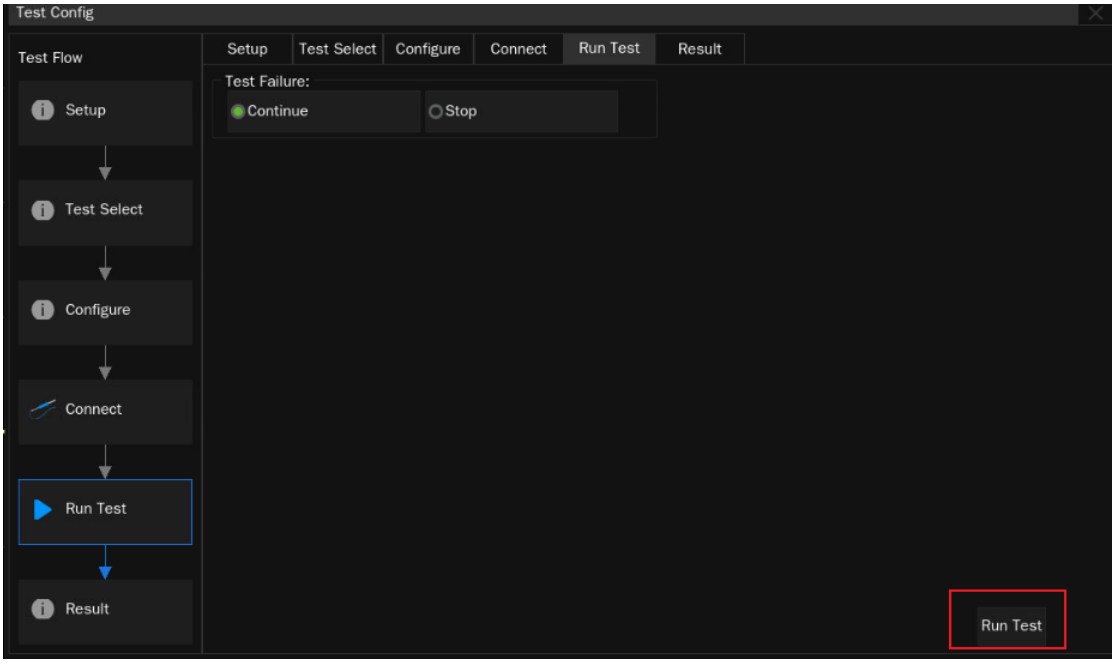


Figure 4-6 Run test window

In the following test process, according to the pop-up window prompts to complete the test. After all test items are completed, the test result window will pop up.

If more than one test item is selected in a round of testing, if there are different connection methods, there will be a pop-up window prompting the connection method of the test item before the next item is carried out, after changing the connection environment, click **Run Test** in the pop-up window to continue the test.

4.2 View Test Results

Click " **Result** " to view the corresponding test results.

The upper half of the test results window contains the test items, outlining the results of every test item, as well as the pass thresholds, as shown in Figure 4-7.

The lower half of the test result window is the corresponding detail waveform, click on the item you are concerning in the upper half of the test results window, and the corresponding details will be displayed in the lower half of the window, click on the picture to see the details of the test waveform in a large view, as shown in Figure 4-8.

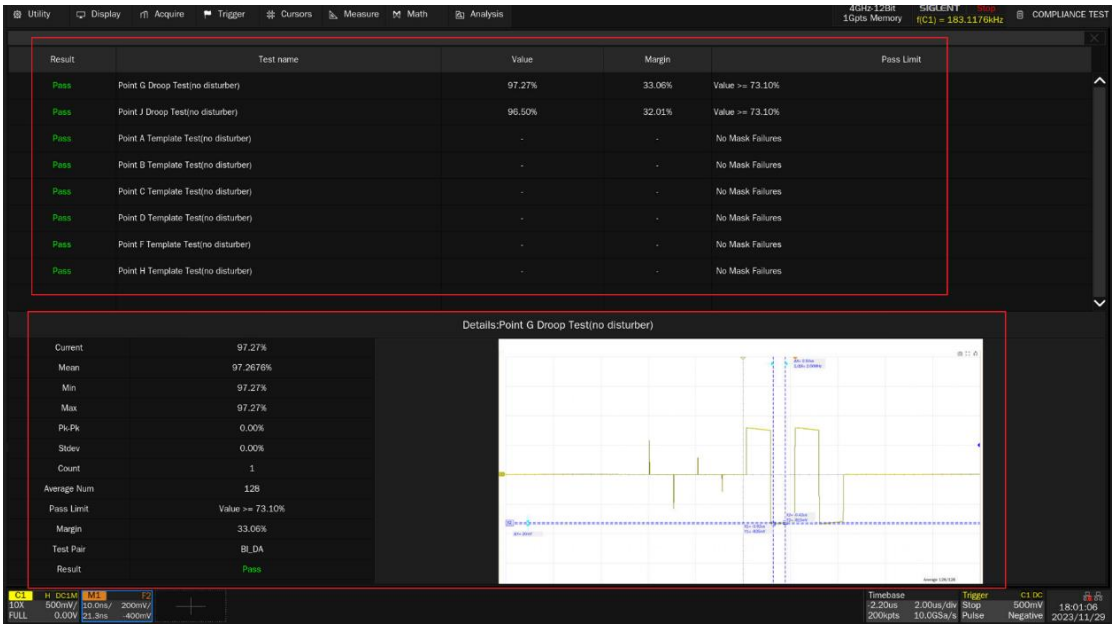


Figure 4-7 List of Test Items

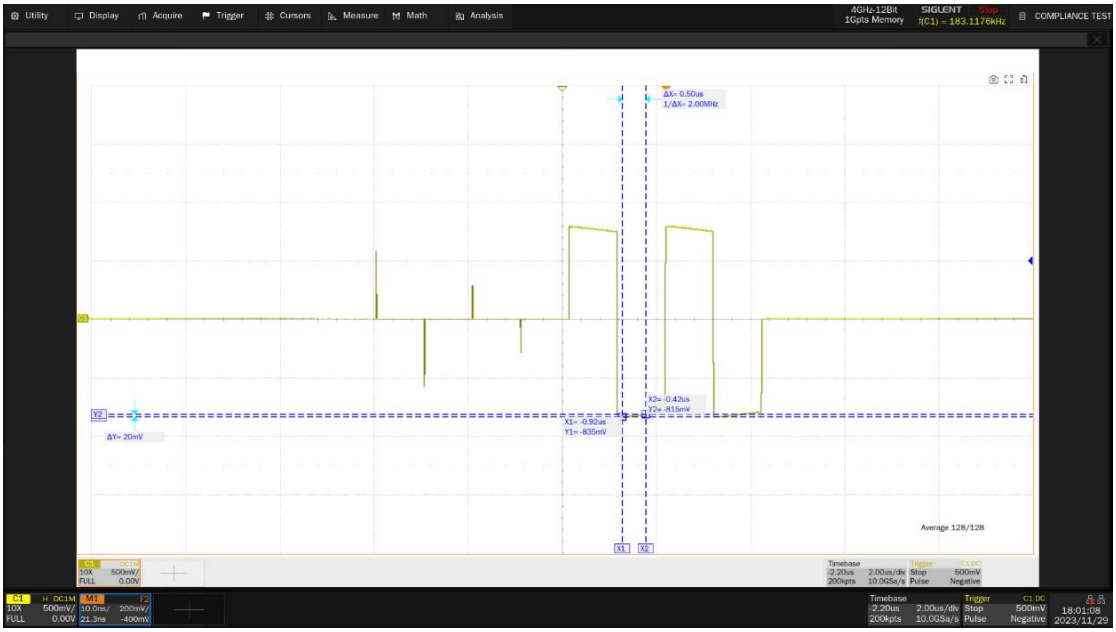


Figure 4-8 Waveform details

4.3 Report Setting

Click **Report Setting** , fill in the test information, and select the HTML or XML report type. **Preview Report** can view the generated report in advance. Click **File Management** to select the path to save. Click **Save** to save the test results, as shown in Figure 4-9.

Note: When saved in HTML format, a folder and HTML files will be generated, if you need to copy to new directory, you need to copy both files to the new directory.

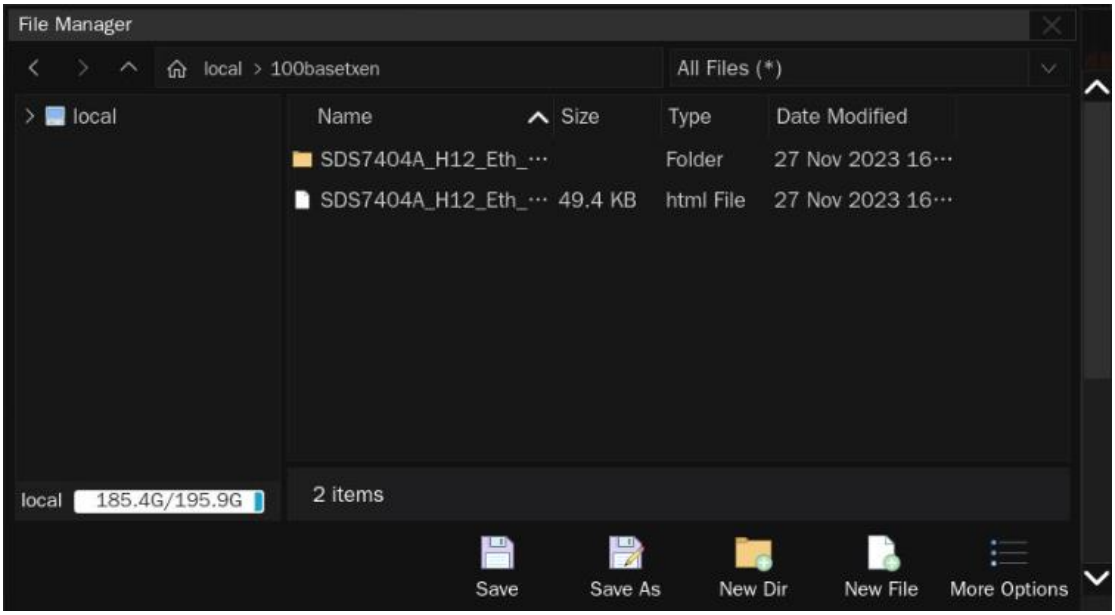
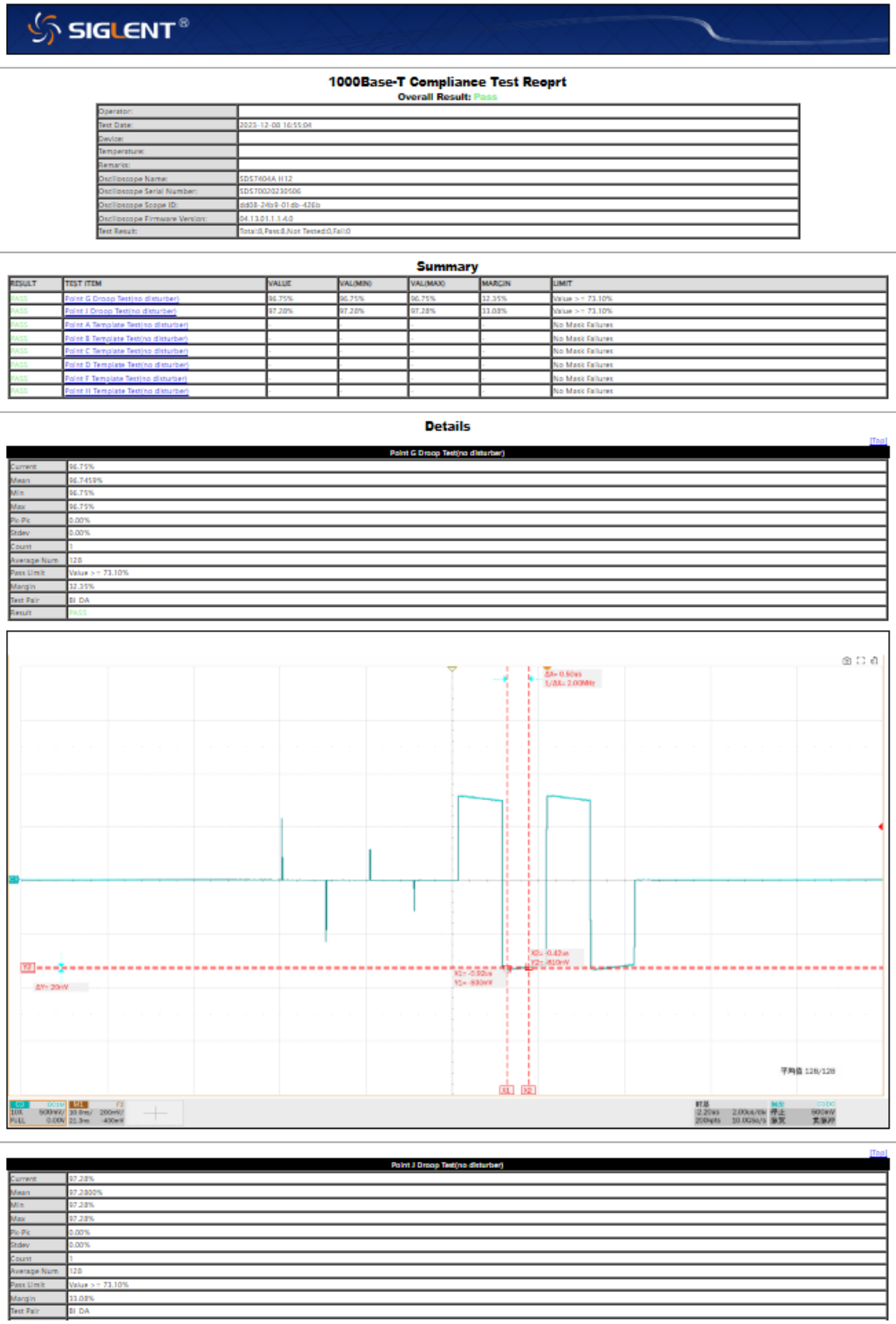


Figure 4-9 Generate report settings

The test report includes a summary table of all test results and with hyperlinks to the details page, which includes a screen shot of the associated test waveform, as shown in Figure 4-10.



1000Base-T Compliance Test Reoprt

Overall Result: Pass

Operator:	
Test Date:	2023-12-08 16:55:04
Device:	
Temperature:	
Remarks:	
Oscilloscope Name:	SDS7404A H12
Oscilloscope Serial Number:	SDS7002023050G
Oscilloscope Scope ID:	6e88-24b9-01db-42Eb
Oscilloscope Firmware Version:	04.13.01.1.1.4.0
Test Result:	Total:8,Pass:8,Not Tested:0,Fail:0

Summary

RESULT	TEST ITEM	VALUE	VAL(MIN)	VAL(MAX)	MARGIN	LIMIT
PASS	Point G Droop Test(no disturber)	96.75%	96.75%	96.75%	12.35%	Value >= 73.10%
PASS	Point J Droop Test(no disturber)	97.28%	97.28%	97.28%	13.08%	Value >= 73.10%
PASS	Point A Template Test(no disturber)			-	-	No Mask Failures
PASS	Point B Template Test(no disturber)			-	-	No Mask Failures
PASS	Point C Template Test(no disturber)			-	-	No Mask Failures
PASS	Point D Template Test(no disturber)			-	-	No Mask Failures
PASS	Point F Template Test(no disturber)			-	-	No Mask Failures
PASS	Point H Template Test(no disturber)			-	-	No Mask Failures

Details

[Top]

Point G Droop Test(no disturber)

Current	96.75%
Mean	96.7459%
Min	96.75%
Max	96.75%
Pk-Pk	0.00%
Stdev	0.00%
Count	1
Average Num	128
Pass Limit	Value >= 73.10%
Margin	12.35%
Test Pair	BI DA
Result	PASS

[Top]

Point J Droop Test(no disturber)

Current	97.28%
Mean	97.2800%
Min	97.28%
Max	97.28%
Pk-Pk	0.00%
Stdev	0.00%
Count	1
Average Num	128
Pass Limit	Value >= 73.10%
Margin	13.08%
Test Pair	BI DA

Figure 4-10 Test Report

5 1000 BASE-T Test Environment and Connectivity

Test environment and connectivity for Peak Output Voltage, Droop, Templates will be described in this chapter.

Test environment and connectivity for Jitter, MDI Return Loss, MDI Common-mode Output Voltage are described in the corresponding chapters.

With or without TX_TCLK, test environment and connectivity is different for Transmitter Distortion tests , which are described in this chapter and in chapter <9 Transmitter Distortion>.

5.1 Test Environment and Connectivity Without Disturber

Peak Output Voltage ,Droop Test, Template Test, Transmitter Distortion(without TX_TCLK) without disturber use the same test environment by using section ① or section ⑥ on the test fixture. DUT transmits the signal of test mode 1 or test mode 4 which can support these tests. An active differential probe or two SMA cables can be used to probe the signal with the test fixture. Connections are shown as follows.

5.1.1 Use SMA Cables to Probe Signal

The connection by using two SMA cables is shown in Figure 5-1 and the connection procedure is as follows:

1. Connect the DUT to the J27 connector on section ⑥ of the test fixture by using a short straight-through UTP cable.
2. According to the pair being tested, using two SMA cables with equal length to connect the corresponding test points {DA(J17,J4), DB(J5, J18), DC(J6, J19), DD(J7, J20)} on section ⑥ of test fixture, and to two input channels which are selected as the “DUT Source” channels in the user interface’s **“Configure”** tab .
3. Connect other unused test points on section ⑥ of the test fixture to 50Ω terminators.

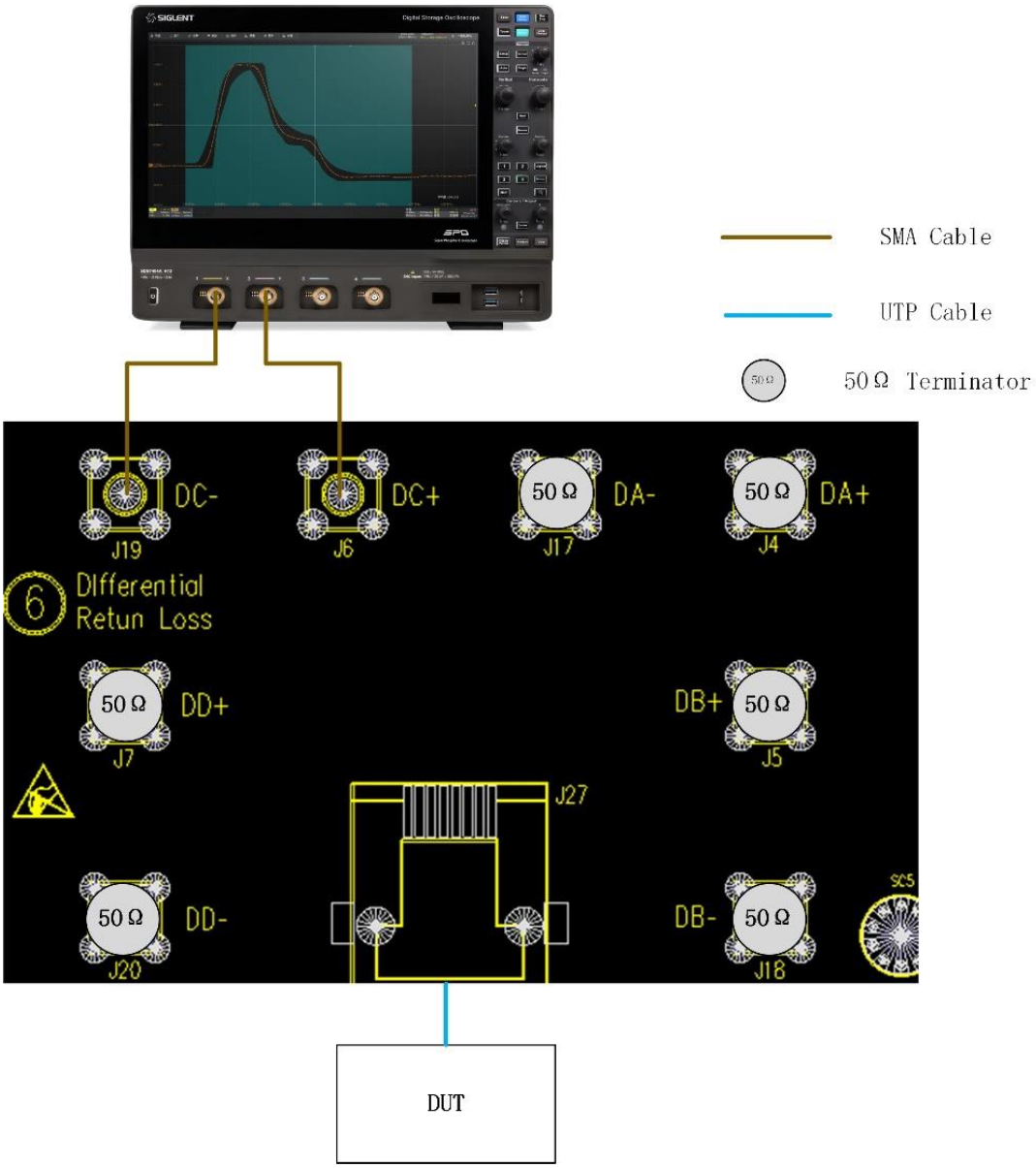


Figure 5-1 Test environment with SMA cables connection, and without disturber

5.1.2 Use a Differential Probe to Probe Signal

The test environment for using an active differential probe to probe 1000 BASE-T of test mode 1 signal and test mode 4 signal (without TX_TCLK and without disturber) is shown in Figure 5-2, and the connection steps are as follows:

(1) Connect the DUT to the J28 connector on section ① of the test fixture by using a short UTP cable;

(2) Connect a differential probe to test point (J1, J10, J21, J25)) on section ① of the test fixture according to the signal pair [(DA+, DA-), (DB+, DB-), (DC+,DC-), (DD+,DD-)] being tested, and to the oscilloscope input channel which is selected as the DUT “Source” channel in the user interface’s **“Configure”** tab.

(3) Ensure correct polarity of the probe head.

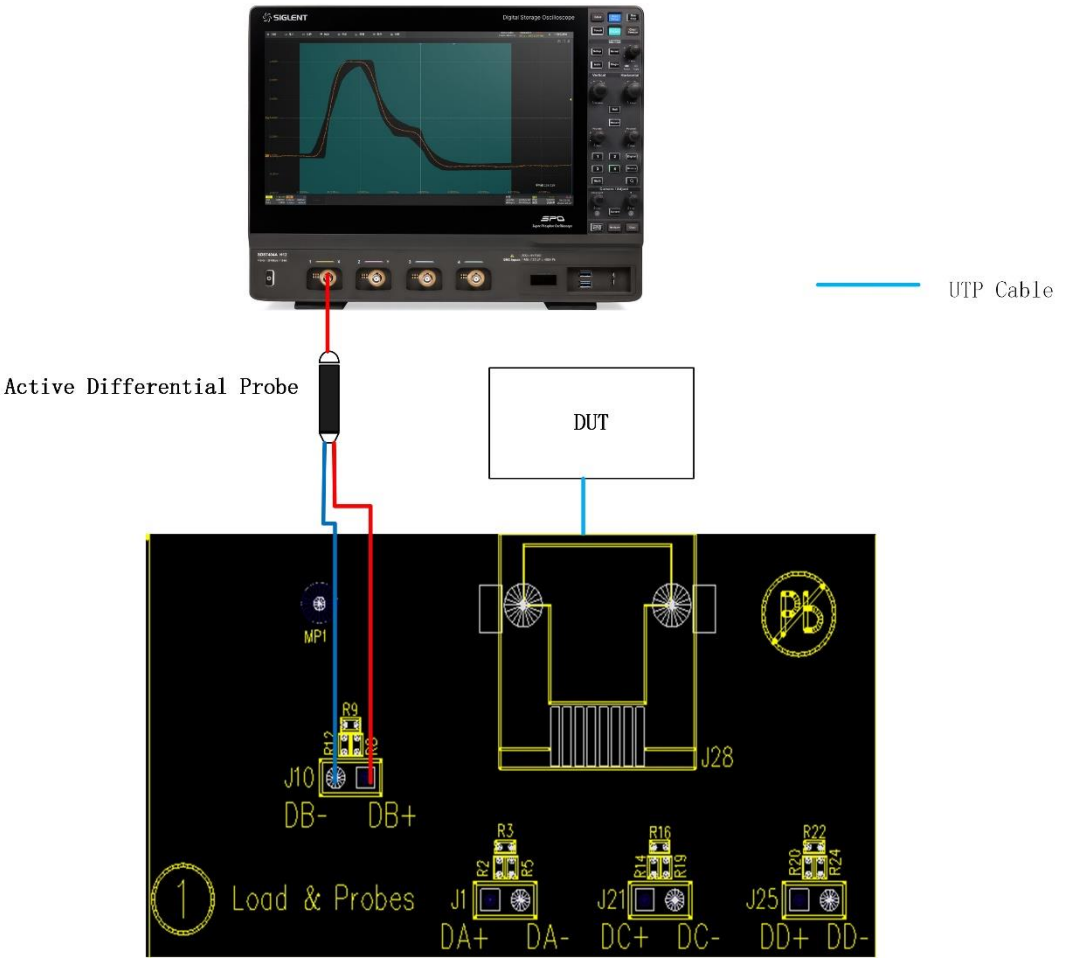


Figure 5-2 Test environment with active differential probe connection, and without disturber

5.2 Test Environment and Connectivity with Disturber

Peak Output Voltage ,Droop Test, Template Test, Transmitter Distortion with disturber but without TX_TCLK using the same test environment by using section ④ on the test fixture. DUT is configured to output the test mode 1 or test mode 4 signal to support these tests.

The test fixture supports probing signal with SMA cables.

Before running tests with disturbing signal, it is necessary to complete the calibration of the test fixture, including the calibration of the DUT signal path and the calibration of disturbing signal path. After completing the test fixture calibration, you can start the test.

5.2.1 The Test Circuit Design with Disturber on the Test Fixture

On the test fixture, the circuit block diagram for section ④ is shown in Figure 5-3. The types of connectors on section ④ are as follows:

- J64: Ethernet connector, connects to the DUT.
- J65, J81: SMA connectors, connect to the output channels of the arbitrary waveform generator.
- J66, J82: SMA connectors, connect to the input channels of the oscilloscope.
- J71, J59, J76, J84: 2-pin, 2.54mm pitch connectors that supports jumpers to short signals.
- J63, J80: 3-pin, 2.54mm pitch connectors that support jumpers to short signals.

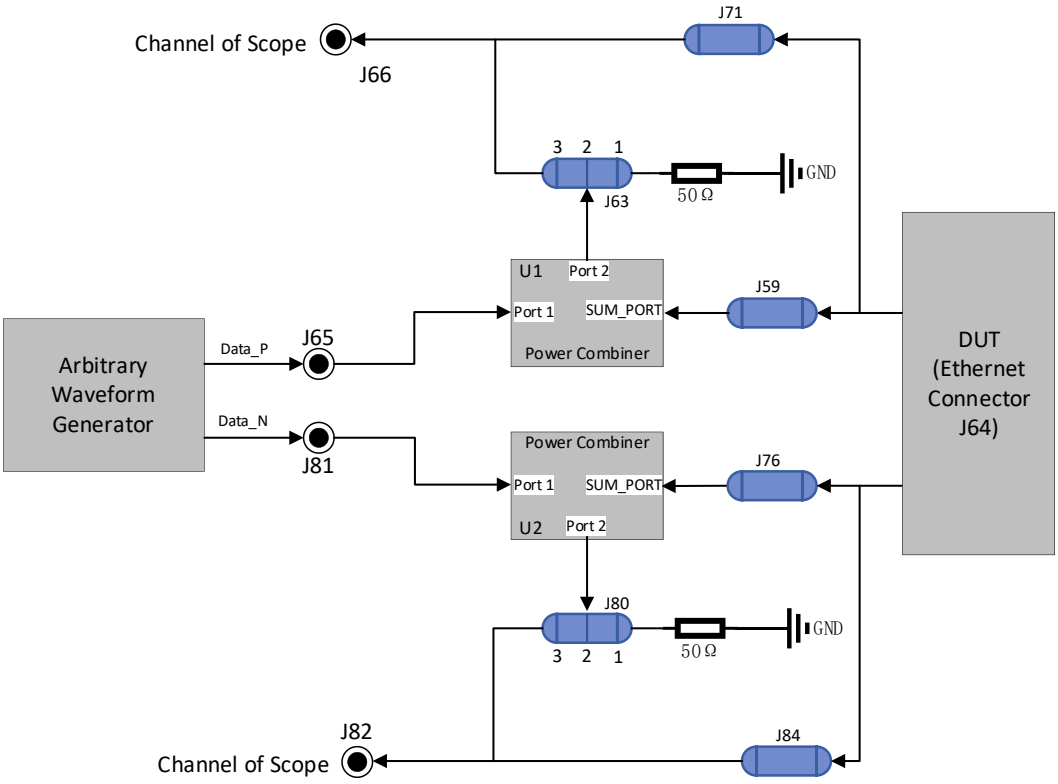


Figure 5-3 The block diagram of circuitry on section ④ of the test fixture

In Figure 5-3, only one of the four pairs of 1000M Ethernet signals can be tested at the same time, the user can install jumpers according to the tested signal pair shown in Table 5-1 and in Figure 5-4.

Table 5-1 Signal Pair Being Tested According to the Installation of Jumpers

Tested Signal Pair / Connection	Pair A		Pair B		Pair C		Pair D	
Jumpers Installation	J60 J67	J69 J75 J79	J73 J77	J62 J75 J79	J61 J68	J62 J69 J79	J74 J78	J62 J69 J75

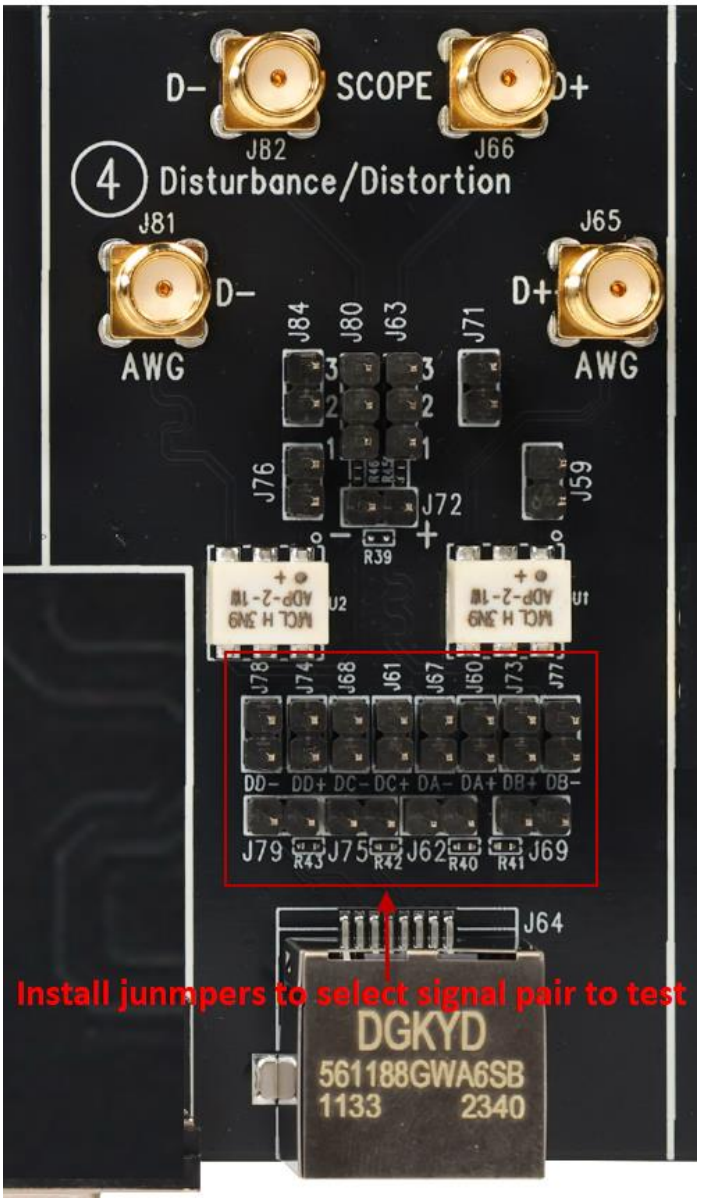


Figure 5-4 Signal Pair Being Tested According to the Installation of Jumpers

5.2.2 DUT Signal Path Calibration

DUT signal path calibration with SMA cables is shown as Figure 5-5 and Figure 5-6, the calibration procedure for signal path is as follows:

(1) Use a short UTP cable to connect the DUT to the J64 connector on section ④ of the test fixture.

(2) Use two SMA cables with equal length to connect the test points J82(D-) and J66(D+) on section ④ of the test fixture to two input channels of the oscilloscope.

(3) J65 and J81 are installed with two 50Ω terminators.

(4) As Table 5-1 shown, select the signal pair being calibrated. For example, for pair A, install jumpers on J60, J67 to connect the Pair A signal to the test circuit. Install jumpers on J69, J75, J79 for 100Ω termination of untested signal pairs.

(5) As Figure 5-5 shown, install jumpers on J71, J84 and remove jumpers from J59, J63, J76, J80. Click **Run Test** on the **Test Config** window, oscilloscope will measure the DUT's raw signal amplitude.

(6) After you confirm the DUT's raw signal amplitude meets requirement, pls click **Next** on the pop-up window, which will continue to test the DUT's signal which is attenuated after pass through the power combiners U1 and U2.

(7) As shown in Figure 5-6, install jumpers on J59, J63 (pin2, 3), J76, J80 (pin2, 3) and remove jumpers from J71, J84. Oscilloscope measures the DUT's signal amplitude which goes through the power combiners. Click the **Complete** after confirming that the amplitude measurement meets the requirements.

(8) The oscilloscope divides the raw signal amplitude of the DUT and the signal amplitude which is attenuated by the power combiners to obtain the amplitude attenuation coefficient. The signal path calibration is finished.

Note: The attenuation coefficient of the power combiner is about 0.7, so the amplitude attenuation coefficient after calibration is about 1.43.

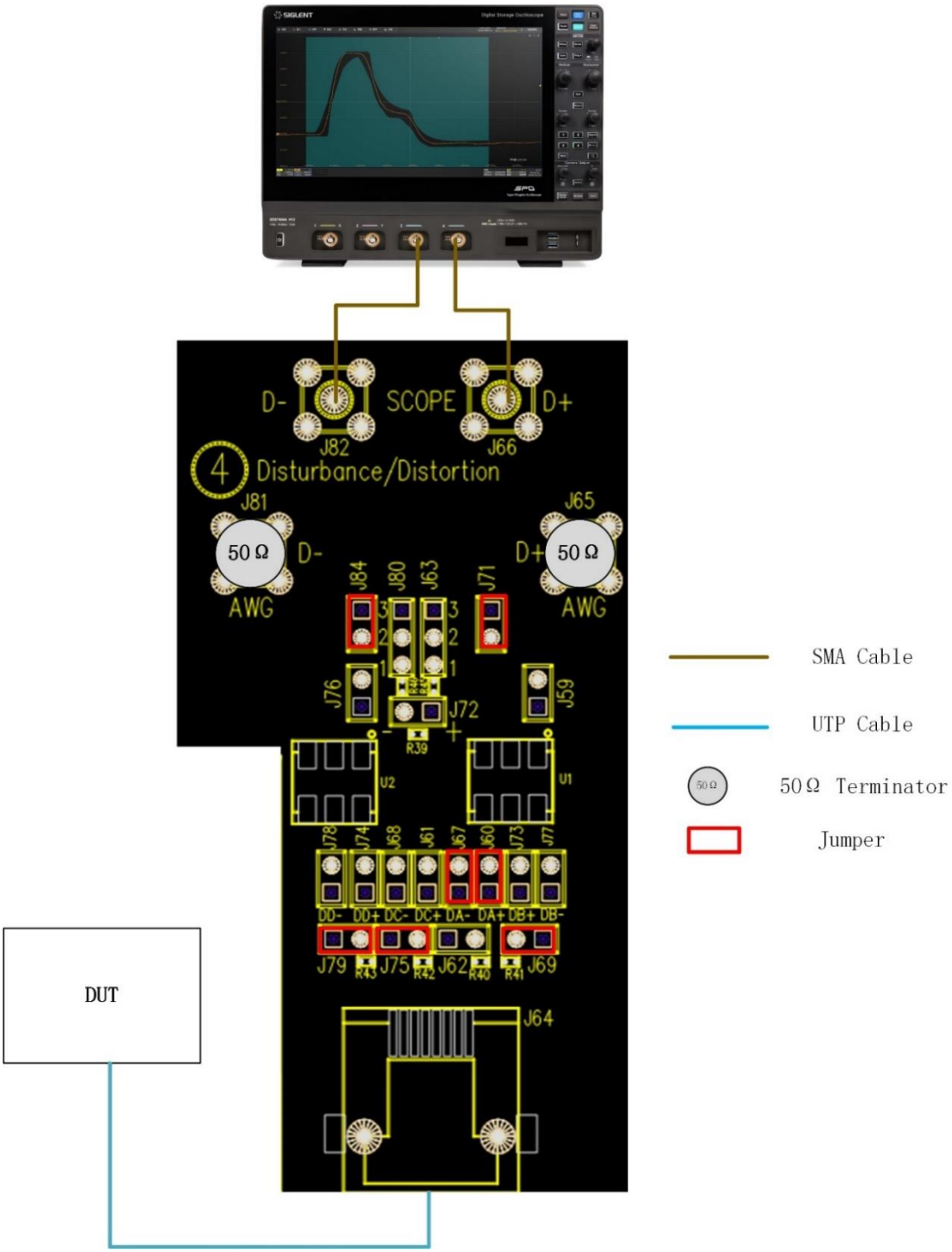


Figure 5-5 Oscilloscope measures the DUT's raw signal

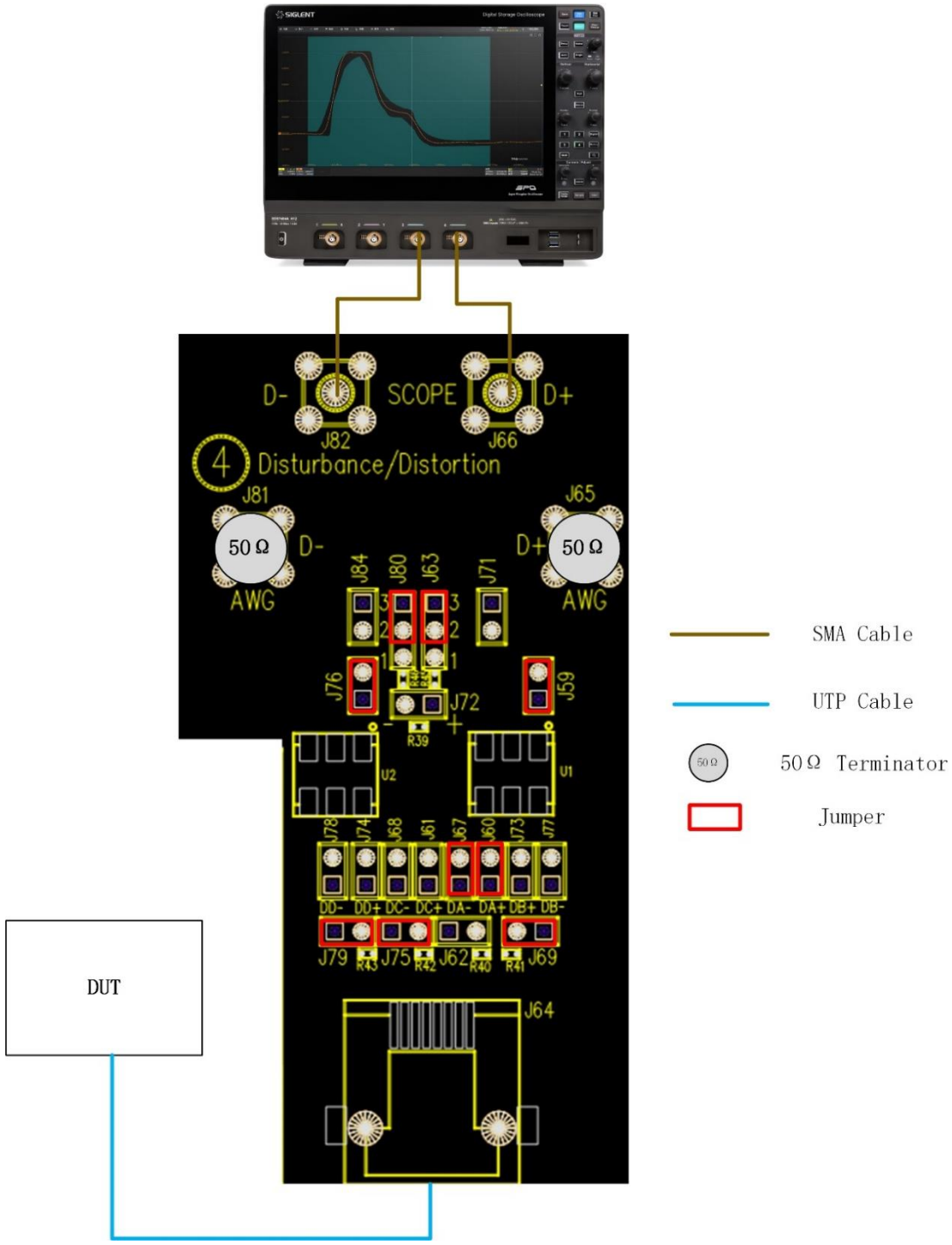


Figure 5-6 Oscilloscope measures DUT's signal amplitude which pass through the power combiners

If the test fixture has been calibrated, and the attenuation coefficient of the signal path is already known, when the user tests different signal pairs (Pair A/B/C/D), in order to simplify the test procedure, the coefficient can also be manually filled through **Configure** -> **Calibration Setup** -> **Amplitude attenuation coefficient** -> **Coefficient** which is shown in Figure 5-7. In the calibration step, and In the pop-up window of **Fixture Calibration** , click **Skip** or **Cancel Test** and oscilloscope will use the default coefficient to do the tests.

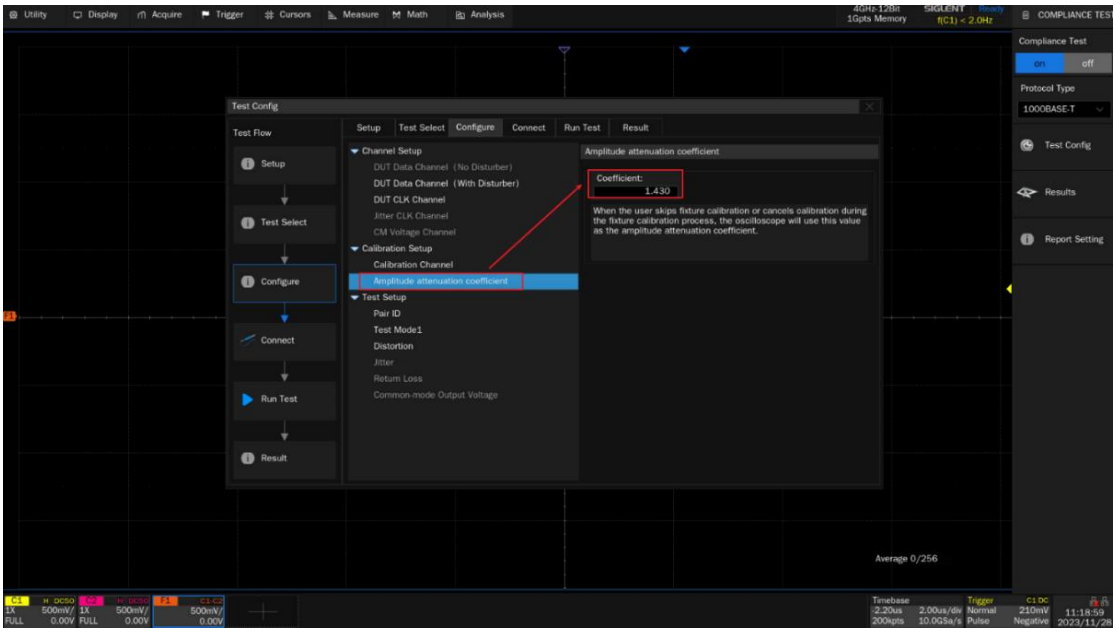


Figure 5-7 Amplitude attenuation coefficient window

5.2.3 Disturber Signal Path Calibration

Disturber path calibration is shown as Figure 5-8, the calibration procedure is as follows:

(1) Disconnect the DUT to the J64 connector on section ④ of the test fixture.

(2) Install jumpers on J59, J71, J76, J84, J63 (pin1, 2), J80 (pin1, 2).

(3) Adjust the amplitude and frequency of the dual-channel Arbitrary Waveform Generator to output two sine waves with the same amplitude but a 180° phase shift.

(4) The oscilloscope subtracts two input signals to obtain the differential disturbing signal amplitude. The differential amplitude should meet the requirement shown as

(5) Table 5-2.

(6) Recode the value of the Arbitrary Waveform Generator voltage setting.

Table 5-2 The requirements of disturbing signal frequency and amplitude

Test Mode	Disturbing Signal Frequency	Disturbing Signal Amplitude at DUT
Test Mode 1	31.25MHz	2.8 Vp-p
Test Mode 4	20.833MHz	5.4 Vp-p

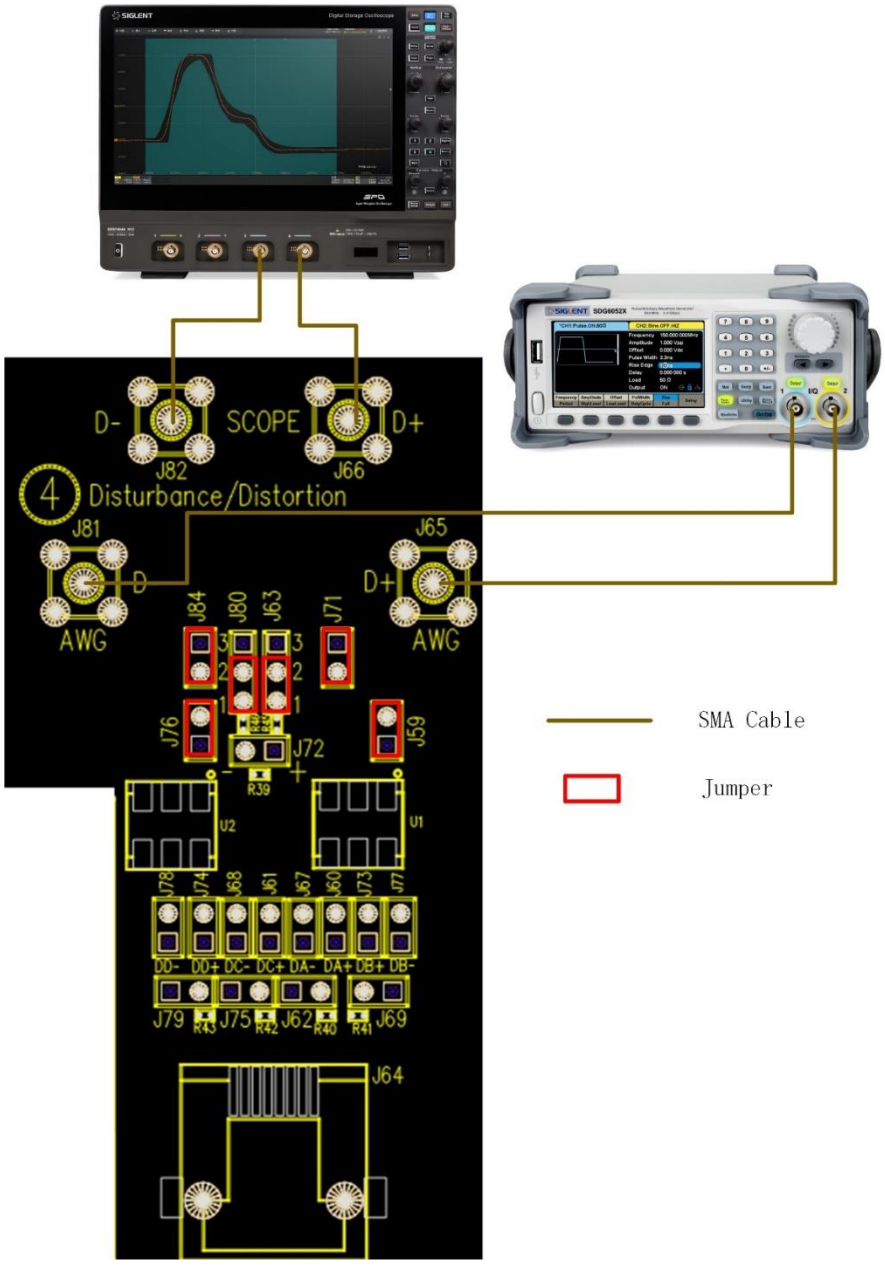


Figure 5-8 Disturber signal path calibration

5.2.4 Connection for Test Mode 1 and 4 When Doing Compliance Test

Connection for peak output voltage, droop, template, transmitter distortion measurement with disturbing signal and without TX_TCLK is shown as Figure 5-9, the measurement procedure is as follows:

(1) Use a short UTP cable to connect the DUT to the J64 connector on section ④ of the test fixture.

(2) Use two SMA cables with equal length to connect the test points J82(D-) and J66(D+) on section ④ of the test fixture to two input channels on the oscilloscope.

(3) Use two SMA cables with equal length to connect the test points J81(D-) and J65(D+) on section ④ of the test fixture to two output channels of the Arbitrary Waveform Generator.

(4) As Table 5-1 shown, select the signal pair being test. For example, for pair A, install jumpers on J60, J67 to connect the signal Pair A to the test circuit. Install jumpers on J69, J75, J79 for 100Ω termination for the signal pairs not being tested. For the signal pair (Pair B/C/D) being tested, install the jumpers as Table 5-1 shown.

(5) Install jumpers on J59, J63 (pin2, 3), J76, J80 (pin2, 3) and remove jumpers from J71, J84. Oscilloscope measures the DUT's signal amplitude which pass through the power combiners U1 and U2.

(6) Configure the DUT to output the Test Mode 1 or Test Mode 4 signal and set the Arbitrary Waveform Generator to output the corresponding disturbing signal which has finished calibrating.

(7) Oscilloscope captures the signal, analyzes and processes it to obtain the measurement results.

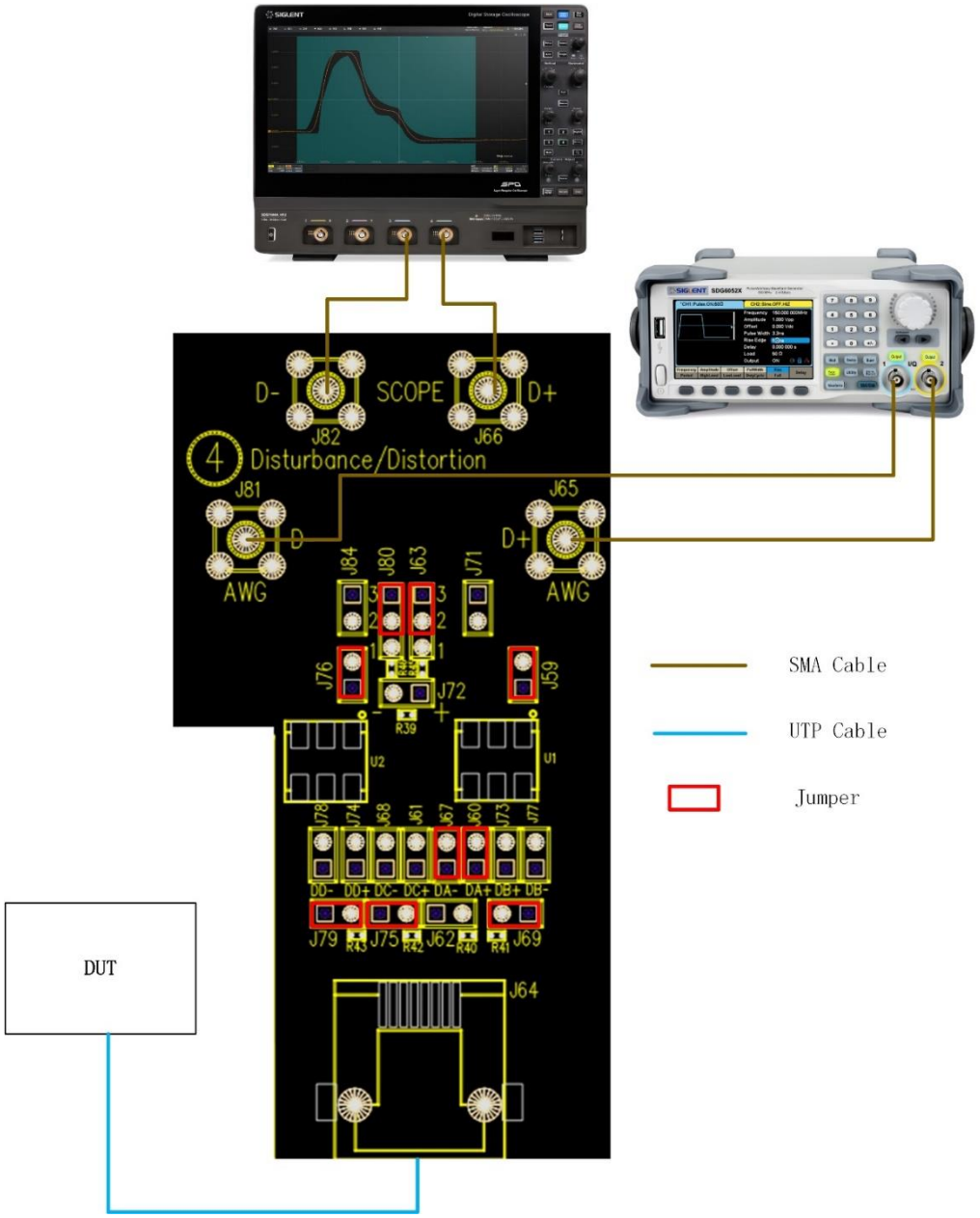


Figure 5-9 Test mode 1 and 4 test environment with disturber

6 Peak Output Voltage Tests

6.1 Test Waveform and Standard Reference

When the DUT is in test mode 1, with or without disturbing signals, Peak Output Voltage is used to verify whether the signal level from the DUT output port is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.1. These tests measure the output voltage of points A, B, C, and D of the Test Mode 1 signal at the MDI. The waveform for test mode 1 is shown in Figure 6-1, and this test waveform is also used for Droop and Templates tests.

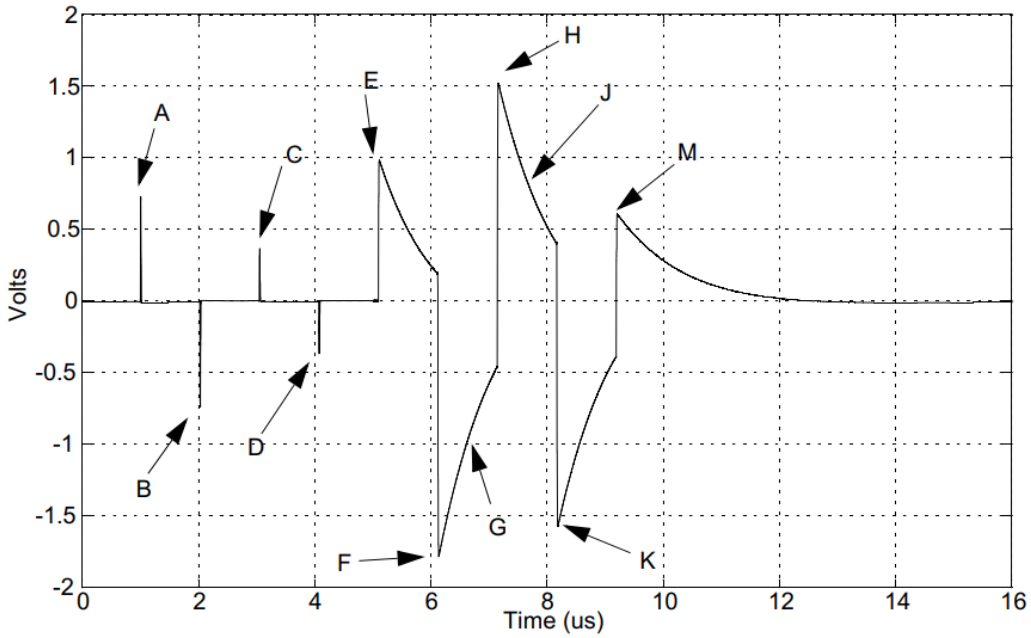


Figure 6-1 Example of transmitter test mode 1 waveform (1 cycle)

According to the IEEE 802.3, Subclause 40.6.1.2.1 specification, the allowable ranges for Peak Output Voltage Measurements are shown as Table 6-1.

Table 6-1 Allowable Ranges for Peak Output Voltage Measurements

Test Item	Allowable Range
Point A Peak Output Voltage	Absolute value of Peak A is 670mV~820mV
Point B Peak Output Voltage	Absolute value of Peak B is 670mV~820mV
Difference A and B	The absolute value of the peak of the waveforms at points A and B shall differ by less than 1% from the average of the absolute values of the peaks of the waveform at points A and B
Point C Peak Output Voltage	Absolute value of Peak C is within 2% of 1/2 the average amplitude of Peaks A and B
Point D Peak Output Voltage	Absolute value of Peak D is within 2% of 1/2 the average amplitude of Peaks A and B

Test Purpose:

- To test whether the MDI interface has the enough power to transmit the signal for 100 meters.
- To test whether the rise time is fast enough to allow rapid data exchange.
- To test whether the MDI interface emits excessive interference signal that exceeds FCC Class A requirements.
- To test whether the signal is symmetrical, which are points A, B and points C, D are symmetrical or not.

6.2 Algorithm

Standard reference is IEEE 802.3-2018, Subclause 40.6.1.2.1.

After configuring the DUT to output the Test Mode 1 signal, oscilloscope will apply a 2MHz high-pass filter in the software after acquiring the data, and measure peak voltage at Point A, B, C, or D.

The peak output voltage allowable range for point A and B is: the absolute value is within 670mV~820mV (750mV±0.83dB).

The calculation and passing criteria for difference A and B is:

|(|Peak A or B| - (|Peak A| + |Peak B|)/2) / ((|Peak A| + |Peak B|)/2)| * 100%≤1%

Allowable range for point C and D peak output voltage is: Absolute value of Peak C or D is within 2% of 1/2 the average amplitude of Peaks A and B. The calculation is as follows:

$$|\text{Point C or D}| \geq (1-2\%) \times \frac{1}{2} \times [\,(|\text{Peak A}| + |\text{Peak B}|)/2]$$

and

$$|\text{Point C or D}| \leq (1+2\%) \times \frac{1}{2} \times [\,(|\text{Peak A}| + |\text{Peak B}|)/2]$$

6.3 Peak Output Voltage Tests Without Disturber

The peak output voltage tests can be implemented with or without disturbing signals.

The peak output voltage tests environment without disturber is described in this chapter.

6.3.1 Test Environment and Connectivity

Test environment and connection for peak output voltage tests, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

6.3.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **No Disturber** > **Peak Output Voltage (IEEE802.3-2018, 40.6.1.2.1)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.
(4) Check the correctness of the test environment setup in the **Connect** tab.
(5) Click **Run Test** .
(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and applies a 2MHz high-pass filter in the software after acquiring the data. After finishing the tests will output the test results.

6.4 Peak Output Voltage Test with Disturber

Peak output voltage test with disturber needs to use the section ④ on the test fixture. Arbitrary Waveform Generator needs to output two sine waves with the frequency of 31.25MHz but a 180° phase shift and the amplitude of the difference signal of two sine waves is 2.8Vp-p at the DUT.

6.4.1 Test Environment and Connectivity

Before running tests with disturbing signal, it is necessary to complete the calibration of the text fixture for DUT signal path and disturbing signal path, after calibration, you can implement the peak output voltage tests with disturber, please refer to <5.2 Test Environment and Connectivity with Disturber>.

6.4.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.
(2) In **Test Select** label to select the test items, the step is **Test Select** > **with Disturber** > **Peak Output Voltage (IEEE802.3-2018, 40.6.1.2.1)** .
(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.
(4) Check the correctness of the test environment setup in the **Connect** tab.
(5) Click **Run Test** .
(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and applies a 2MHz high-pass filter in the software after acquiring the data. After finishing the tests will output the test results.

6.5 Test Results Reference

The test results of peak output voltage are shown as Figure 6-2.

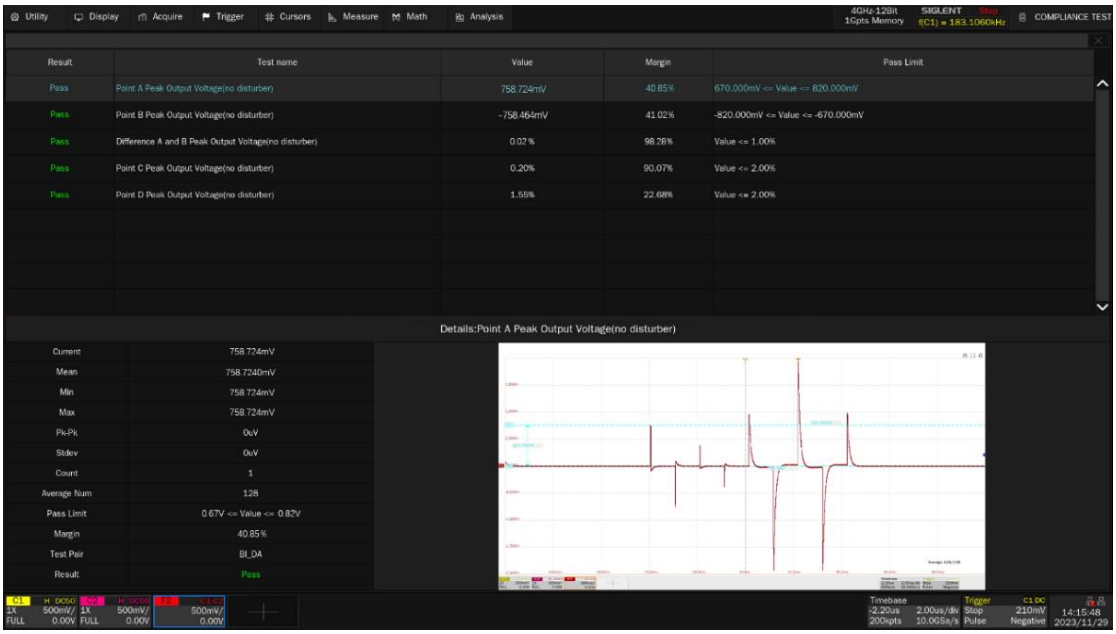


Figure 6-2 Test results for peak output voltage

The details of the test waveform for peak output voltage are shown as Figure 6-3.

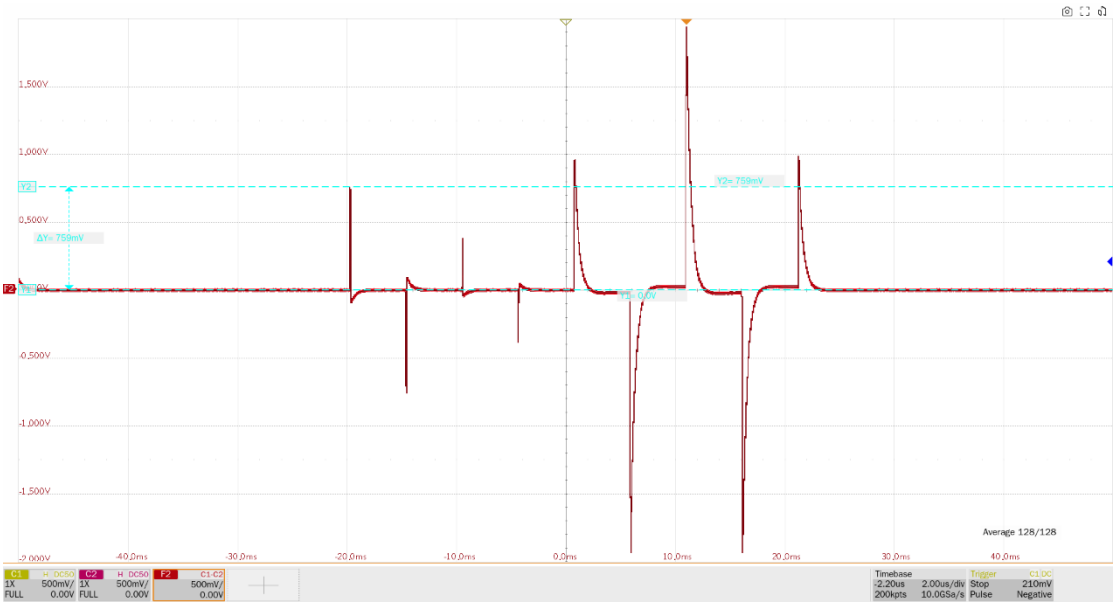


Figure 6-3 Waveform details for peak output voltage tests

7 Droop Tests

7.1 Test Waveform and Standard Reference

When the DUT is in test mode 1, with or without disturbing signals, droop tests are used to verify whether the output droop of differential signal from the DUT MDI port is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.2. Voltage is measured at points F and G, and at points H and J of the Test Mode 1 signal, as indicated in Figure 6-1. The amplitude of the peak voltage at points G and J shall be greater than 73.1% of the amplitude of the peak voltage at points F and H respectively. Point G is defined as the point exactly 500ns after point F. Point J is defined as the point exactly 500ns after Point H. This test does not use a high-pass filter.

Droop tests is used to verify that whether the insertion loss is within the requirement.

7.2 Algorithm

The droop tests are calculated as follows:

1. Measure the minimum/ maximum peak voltage at point F and H as shown in Figure 6-1 respectively and define this as Vpeak_F or Vpeak_H after capturing the waveform.
2. Measure the voltage at exactly 500ns after point F or point H as shown in Figure 6-1 respectively and define this as V_G or V_J.
3. Measure the droop percentage of point G to point F, and percentage of point J to point H as:
   % of G = 100%*V_G/Vpeak_F
   % of J = 100%*V_J/Vpeak_H

According to the standard reference in IEEE802.3-2018, Subclause 40.6.1.2.2, the amplitude of the peak voltage at points G and J shall be greater than 73.1% of the amplitude of the peak voltage at points F and H respectively. This test does not use a high-pass filter.

7.3 Droop Tests Without Disturber

The droop tests can be implemented with or without disturbing signals.

The droop tests environment without disturber is described in this chapter.

7.3.1 Test Environment and Connectivity

Test environment and connection for droop tests, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

7.3.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **No Disturber** > **Droop (IEEE802.3-2018, 40.6.1.2.2)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and no pass filter is applied in the software after acquiring the data. After finishing the tests will output the test results.

7.4 Droop Tests with Disturber

7.4.1 Test Environment and Connectivity

Before running tests with disturbing signal, it is necessary to complete the calibration of the text fixture for DUT signal path and disturbing signal path, after calibration, you can implement the droop tests with disturber, please refer to <5.2 Test Environment and Connectivity with Disturber>.

7.4.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **with Disturber** > **Droop (IEEE802.3-2018, 40.6.1.2.2)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and no pass filter is applied in the software after acquiring the data. After finishing the tests will output the test results.

7.5 Test Results Reference

The test results of droop tests are shown as Figure 7-1.

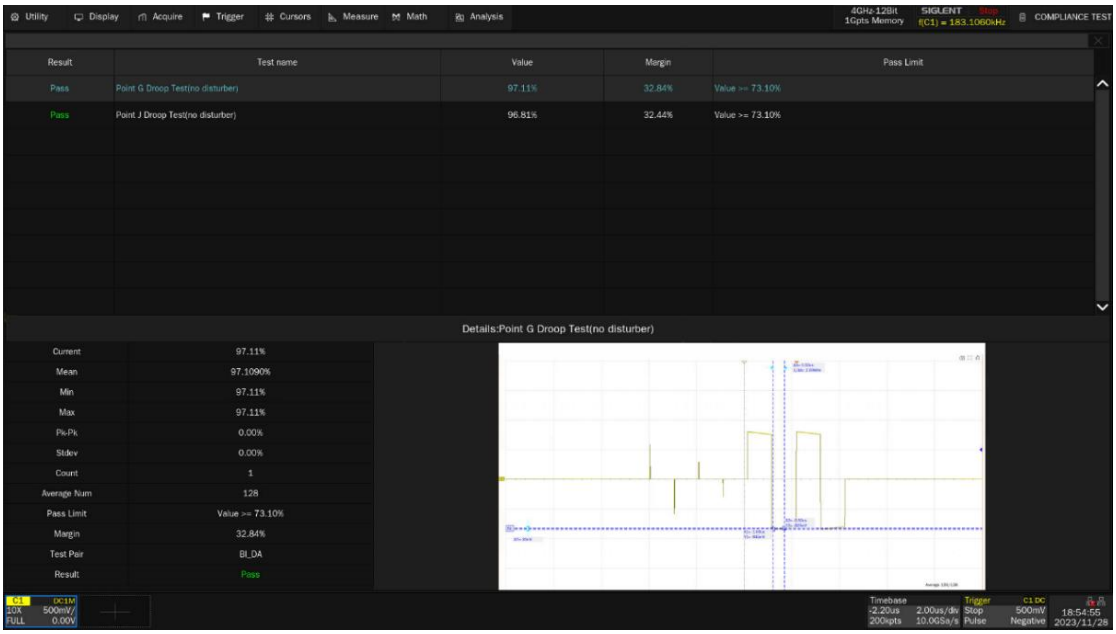


Figure 7-1 Test results of Droop

The details of the test waveform for droop tests are shown as Figure 7-2.

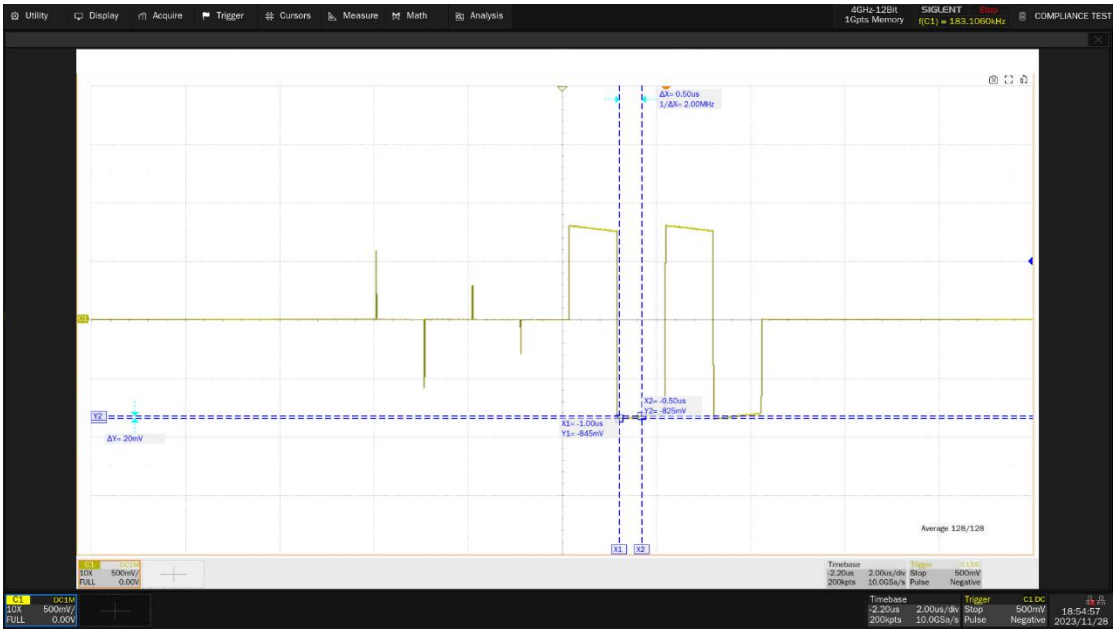


Figure 7-2 Waveform details of droop tests

8 Templates Tests

8.1 Test Waveform and Standard Reference

When the DUT is in test mode 1, with or without disturbing signals, templates tests are used to verify whether the DUT MDI signal is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.3.

8.2 Algorithm

Templates tests ensure that the normalized waveform of the Test Mode 1 signal at points A, B, C, D, F, and H as defined in Figure 6-1 and measured at the MDI after being filtered by a 2 MHz high-pass filter, lies within the time domain templates defined in IEEE802.3-2018, Subclause 40.6.1.2. 3.

The waveform around point A is normalized by dividing by the peak value of the waveform at A. Normalize the waveforms around point B, C, D, F, H are as indicated in Table 8-1.

Table 8-1 Normalize Method in Templates Tests

Point of Test Mode 1 Signal	Normalize Method
Point A	Normalized by dividing by the peak value of the waveform at A
Point B	Normalized by dividing by the negative of the peak value of the waveform at A
Point C	Normalized by dividing by 1/2 times the peak value of the waveform at A
Point D	Normalized by dividing the negative of 1/2 times the peak value of the waveform at A
Point F	Normalized by dividing by the peak value of the waveform at F
Point H	Normalized by dividing by the negative of the peak value of the waveform at F

Normalize the test waveform and shift it in time for the best fit to the specified mask. If the waveform lies within the template, then the test passes. The use of averaging algorithms for test waveform reduces measurement noise and increases measurement resolution.

The IEEE802.3-2018, Subclause 40.6.1.2.3 specification requires that the normalized waveform around points A, B, C and D, should be within the time domain transmit template defined in Figure 8-1. And the normalized waveform around points F, H, should be within the time domain transmit template defined in Figure 8-2.

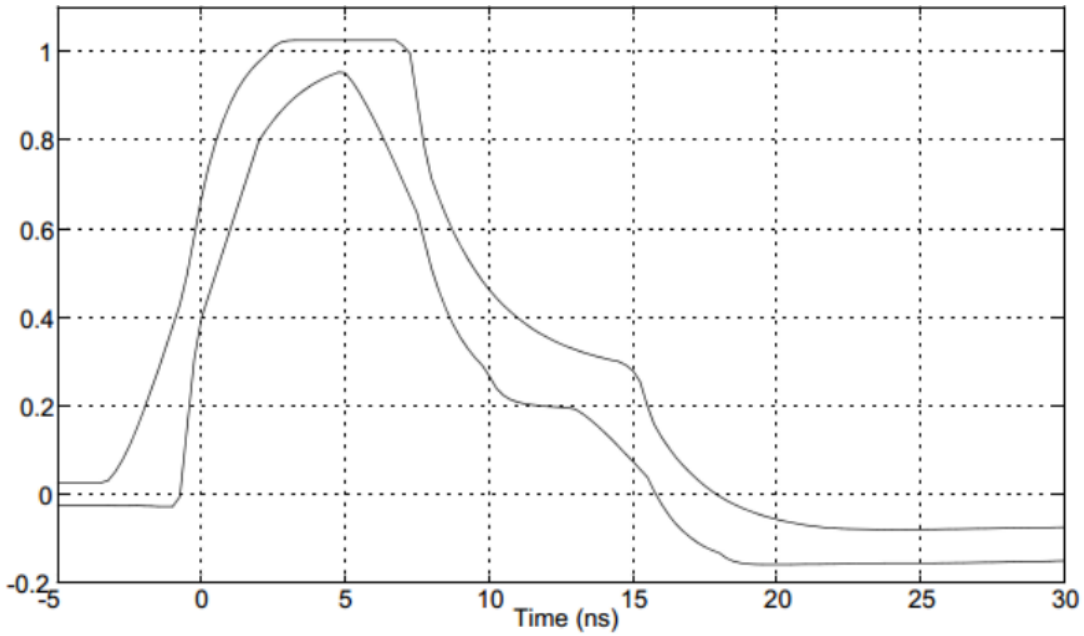


Figure 8-1 Normalized transmit templates as measured at MDI for points A, B, C, D

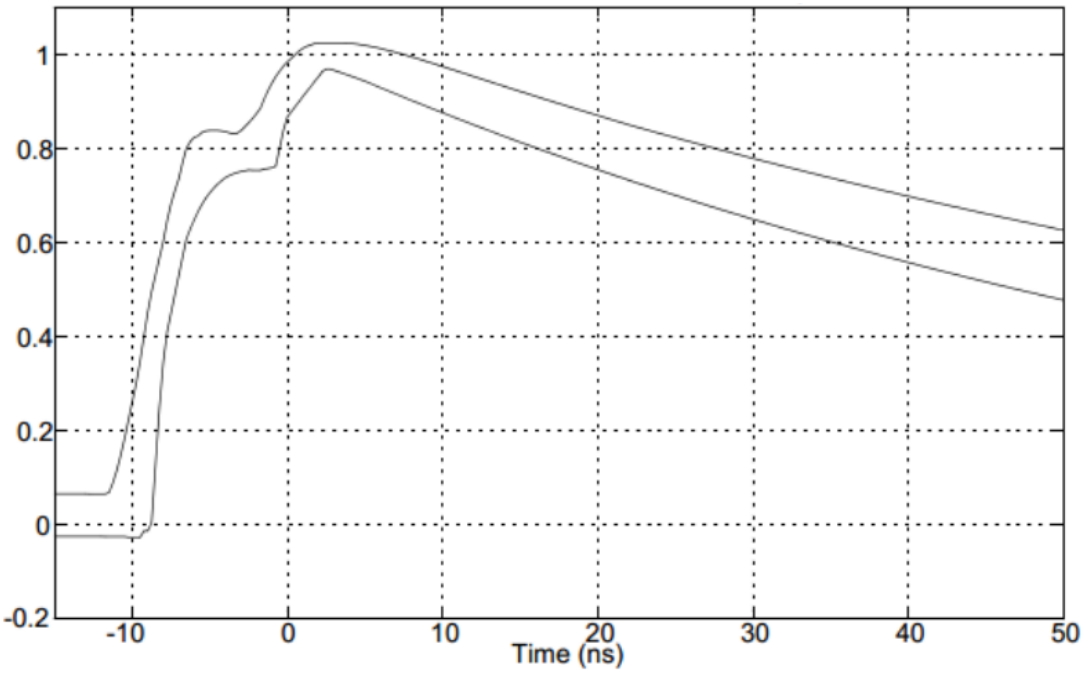


Figure 8-2 Normalized transmit templates as measured at MDI for points F, H

8.3 Templates Tests Without Disturber

The templates tests can be implemented with or without disturbing signals.
The templates tests environment without disturber is described in this chapter.

8.3.1 Test Environment and Connectivity

Test environment and connection for templates tests, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

8.3.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.
(2) In **Test Select** label to select the test items, the step is **Test Select** > **No Disturber** > **Templates (IEEE802.3-2018, 40.6.1.2.3)** .
(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.
(4) Check the correctness of the test environment setup in the **Connect** tab.
(5) Click **Run Test** .
(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and applies a 2MHz high-pass filter in the software after acquiring the data. After finishing the tests will output the test results.

8.4 Templates Tests with Disturber

8.4.1 Test Environment and Connectivity

Before running tests with disturbing signal, it is necessary to complete the calibration of the text fixture for DUT signal path and disturbing signal path, after calibration, you can implement the templates tests with disturber, please refer to <5.2 Test Environment and Connectivity with Disturber>.

8.4.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.
(2) In **Test Select** label to select the test items, the step is **Test Select** > **with Disturber** > **Templates (IEEE802.3-2018, 40.6.1.2.3)** .
(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and applies a 2MHz high-pass filter in the software after acquiring the data. After finishing the tests will output the test results.

8.5 Test Results Reference

The templates tests results for point A, B, C, D is shown as Figure 8-3, Figure 8-4.

The templates test results for point F, H is shown as Figure 8-5, Figure 8-6.

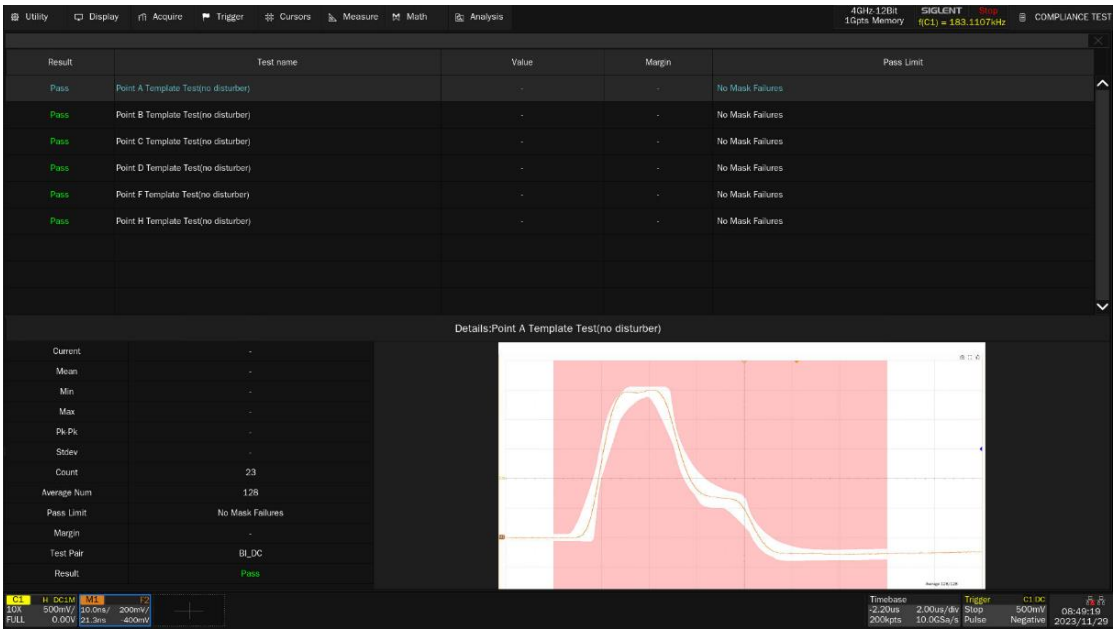


Figure 8-3 Test results reference in templates tests of points A, B, C, D

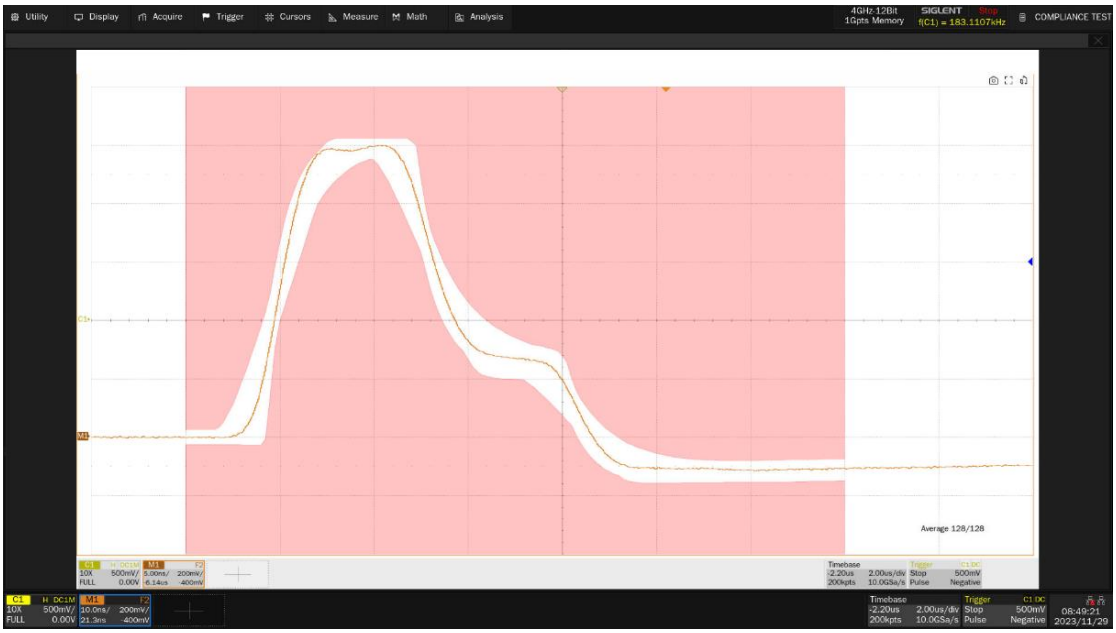


Figure 8-4 Waveform details in templates tests of points A, B, C, D

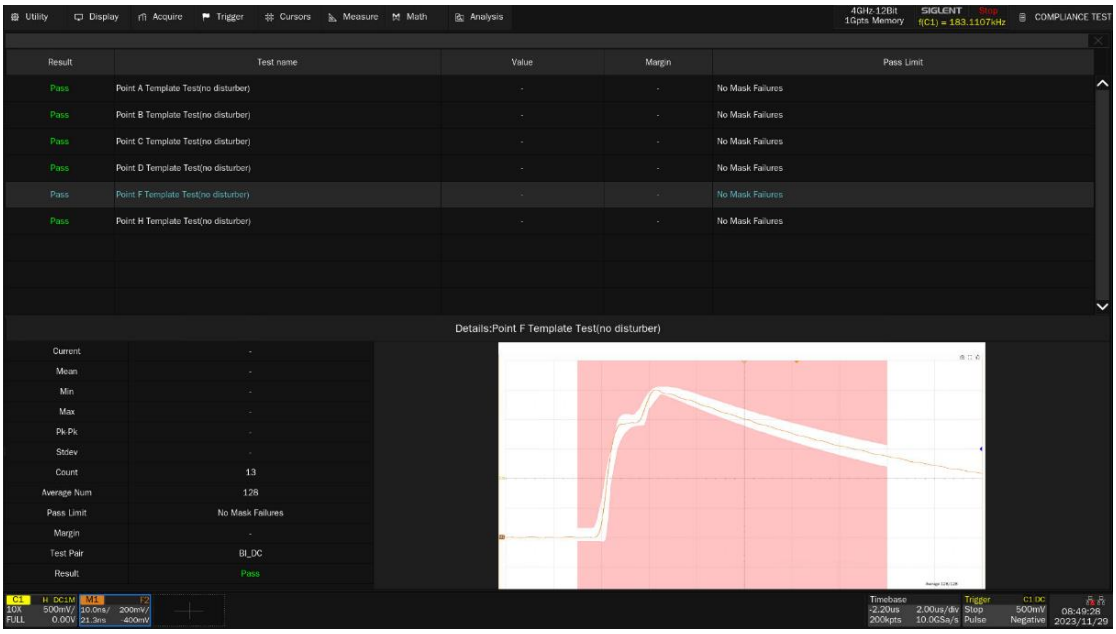


Figure 8-5 Test results reference in templates tests of points F, H

Figure 8-6 Waveform details in templates tests of points F, H

9 Transmitter Distortion Tests

9.1 Test Waveform and Standard Reference

When the DUT is in test mode 4, with or without disturbing signals, peak transmitter distortion tests are used to verify whether the DUT MDI signal is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.4.

When performing the transmitter distortion tests with disturbing signal, the disturber is required to output a 5.4V Vp-p, 20.833MHz sine wave at the DUT.

When in test mode 4, for each pair, with no intervening cable, the peak distortion as defined in IEEE802.3-2018, Subclause 40.6.1.2.4 shall be less than 10 mV.

The peak distortion is determined by sampling the differential signal output with the symbol rate TX_TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the MATLAB code listed in the standard reference or equivalent. Note that this code assumes that the differential signal has already been filtered by the test filter. A PHY is considered to pass this test if the peak distortion is below 10mV for at least 60% of the UI within the eye opening.

Example of Test Mode 4 Waveform is shown as Figure 9-1.

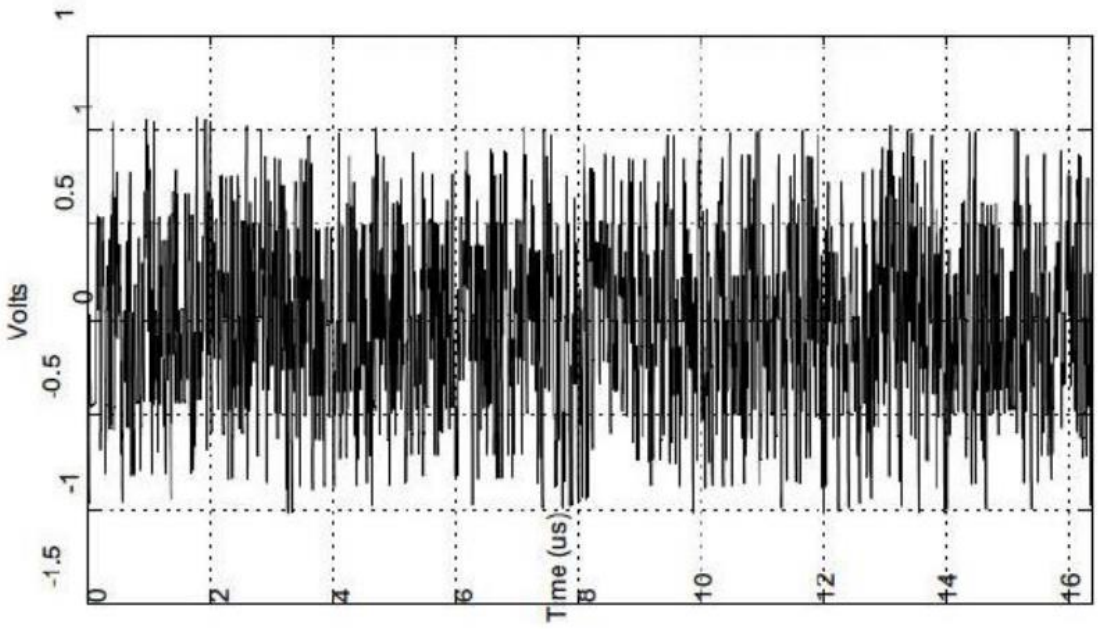


Figure 9-1 Example of Test Mode 4 waveform

9.2 Algorithm

IEEE802.3-2018, Subclause 40.6.1.2.4 describes how transmitter distortion can be measured by analyzing Test Mode 4 signal from a DUT. The steps to analyze the signal is as follows:

(1) Remove the disturbing signal (if it exists).

(2) Compensate for fixture losses.

(3) Apply 2 MHz high-pass filter to the input signal.

(4) Extract the DUT clock.

(5) Calculate the transmitter distortion by using the matlab code provided by IEEE802.3-2018, Subclause 40.6.1.2.4 or equivalent.

9.3 Transmitter Distortion Tests Without Disturber

9.3.1 Transmitter Distortion Tests Without TX_TCLK

9.3.1.1 Test Environment and Connectivity

Test environment and connection for transmitter distortion tests, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

9.3.1.2 Test Procedure

(1) Configure the DUT to output test mode 4 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **No Disturber** > **Transmitter Distortion Without TX_TCLK (IEEE802.3-2018, 40.6.1.2.4)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal by using the same method provided as IEEE802.3-2018, Subclause 40.6.1.2.4 in the software after acquiring the data. After finishing the tests will output the test results.

9.3.2 Transmitter Distortion Tests with TX_TCLK

9.3.2.1 Test Environment and Connectivity

For the transmitter distortion tests without disturber and with TX_TCLK, SMA cables with section ⑥ or an active differential probe with section ① on the test fixture can be used to do the test.

The connection with section ⑥ on the test fixture is shown as Figure 9-2, the test step is as follows:

(1) Using a short UTP cable to connect the DUT to the J27 connector on section ⑥ of the test fixture.

(2) According to the pair being tested, using two SMA cables with equal length to connect the corresponding test points {DA(J17,J4), DB(J5, J18), DC(J6, J19), DD(J7, J20)} on section ⑥ of test fixture to two input channels of the oscilloscope.

(3) Connect other unused test points on section ⑥ of the test fixture to 50Ω terminators.

(4) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

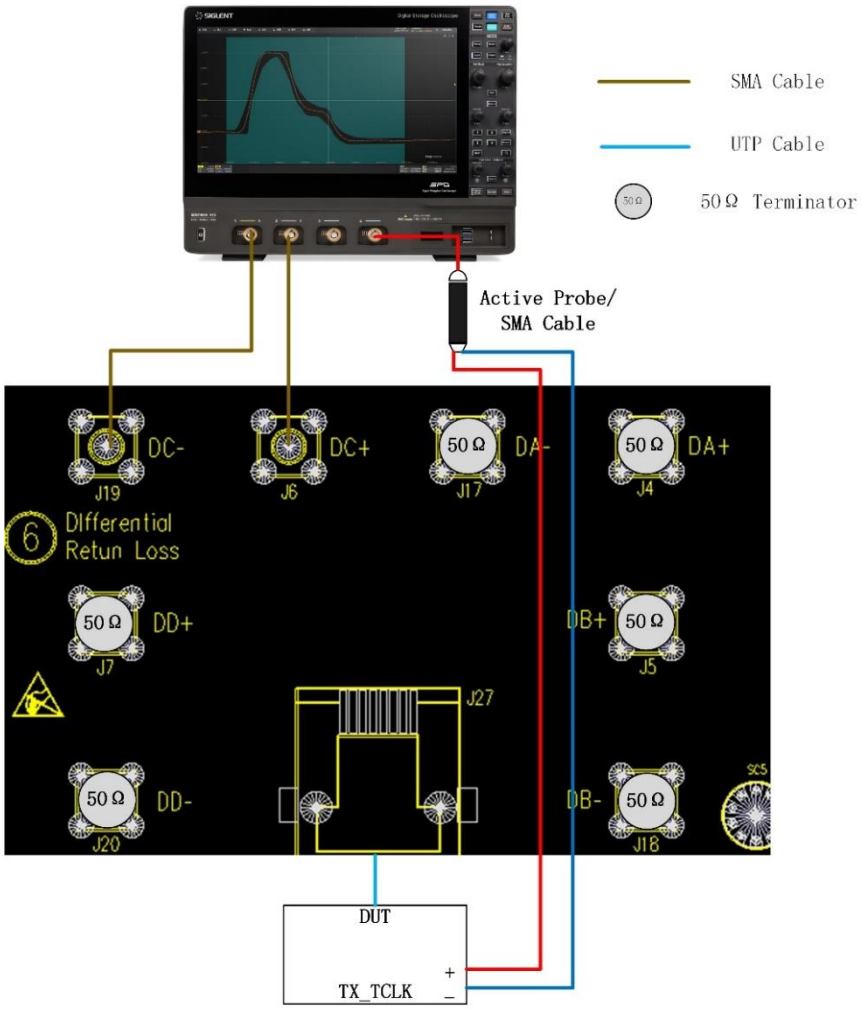


Figure 9-2 Transmitter distortion tests with TX_TCLK and without disturber by using Section ⑥ on the test fixture

The connection with section ① on the test fixture is shown as Figure 9-3, the test step is as follows:

(1) Use a short UTP cable to connect the DUT to J28 connector on section ① of the test fixture.

(2) Use an active differential probe to probe test point (J1, J10, J21, J25) on section ① of the test fixture according to the signal pair being tested {(DA+, DA-), (DB+, DB-), (DC+,DC-), (DD+,DD-)}. Ensure correct polarity of the probe head.

(3) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

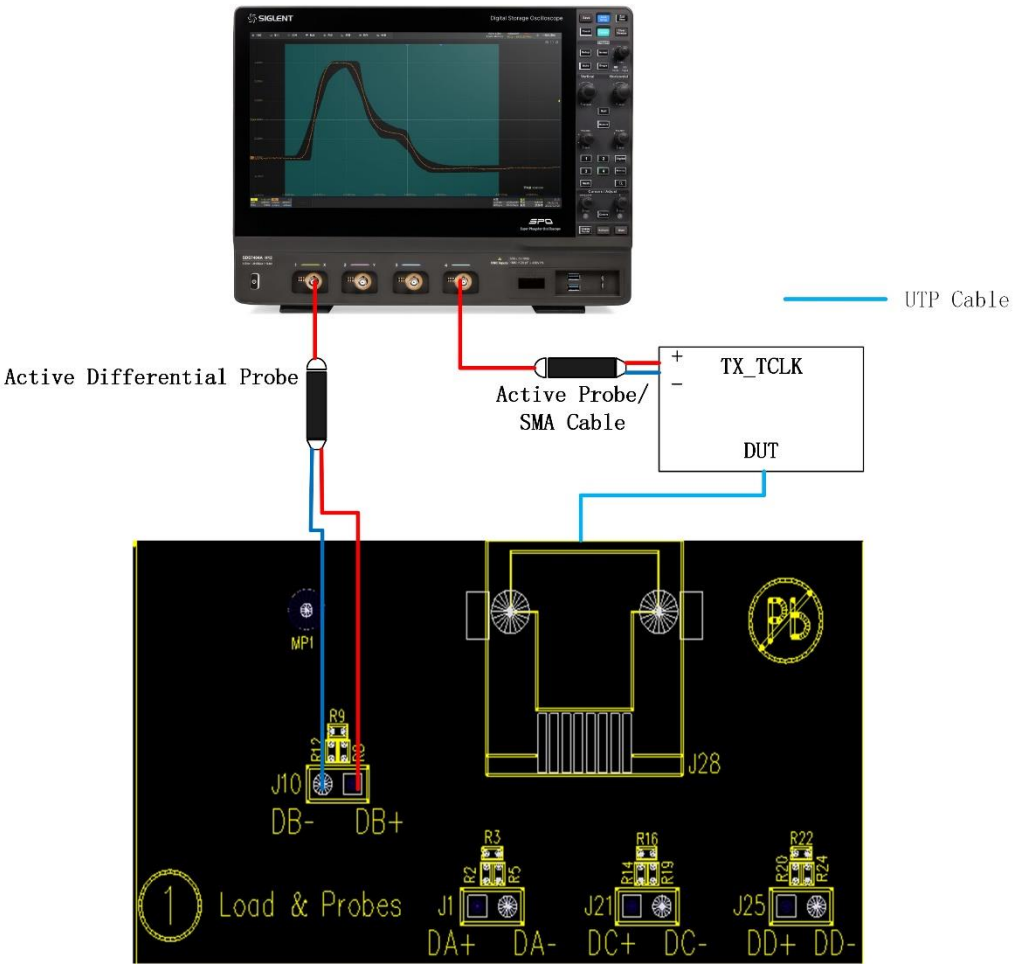


Figure 9-3 Transmitter distortion tests with TX_TCLK and without disturber by using Section ① on the test fixture

9.3.2.2 Test Procedure

(1) Configure the DUT to output test mode 4 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **No Disturber** > **Transmitter Distortion With TX_TCLK (IEEE802.3-2018, 40.6.1.2.4)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal by using the same method provided as IEEE802.3-2018, Subclause 40.6.1.2.4 in the software after acquiring the data. After finishing the tests will output the test results.

9.4 Transmitter Distortion Tests with Disturber

Transmitter distortion with disturber using section ④ on the test fixture to do the test and the waveform generator need to output two 20.833MHz sine waves with the same amplitude but with 180° phase shift, at the DUT, the signal amplitude is 5.4Vp-p.

9.4.1 Transmitter Distortion Tests Without TX_TCLK

9.4.1.1 Test Environment and Connectivity

Before running tests with disturbing signal, it is necessary to complete the calibration of the text fixture for DUT signal path and disturbing signal path, after calibration, you can implement the transmitter distortion tests with disturber, please refer to <5.2 Test Environment and Connectivity with Disturber>.

9.4.1.2 Test Procedure

(1) Configure the DUT to output test mode 4 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **With Disturber** > **Transmitter Distortion Without TX_TCLK (IEEE802.3-2018, 40.6.1.2.4)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal by using the same

method provided as IEEE802.3-2018, Subclause 40.6.1.2.4 in the software after acquiring the data. After finishing the tests will output the test results.

9.4.2 Transmitter Distortion with TX_TCLK

9.4.2.1 Test Environment and Connectivity

Before running tests with disturbing signal, it is necessary to complete the calibration of the text fixture for DUT signal path and disturbing signal path, after calibration, you can implement the transmitter distortion tests with disturber, please refer to <5.2 Test Environment and Connectivity with Disturber>. As Figure 9-4 shown, the transmitter distortion tests with disturber and with TX_TCLK is as follows:

(1) Configure the DUT to output the Test Mode 4 signal.

(2) Use a short UTP cable to connect the DUT to the J64 connector on section ④ of the test fixture.

(3) Use two SMA cables with equal length to connect the test points J82(D-) and J66(D+) on section ④ of the test fixture to two input channels on the oscilloscope.

(4) Using two SMA cables with equal length to connect the test points J81(D-) and J65(D+) on section ④ of the test fixture to two output channels of the Arbitrary Waveform Generator.

(5) As Table 5-1 shown, select the signal pair being tested. For example. for pair A, install jumpers on J60, J67 to connect the signal Pair A to the test circuit. Install jumpers on J69, J75, J79 for 100Ω termination for the signal pairs not being tested. For the signal pair (such as Pair B/C/D) being tested, install the jumpers as Table 5-1 shown.

(6) Install jumpers on J59, J63 (pin2, 3), J76, J80 (pin2, 3) and remove jumpers from J71, J84. Oscilloscope measures the DUT's signal amplitude which pass through the power combiners U1 and U2.

(7) Set the Arbitrary Waveform Generator to output disturbing signals which has finished calibrating. At the DUT, two 20.833MHz sine waves with 180° phase shift is subtracted, the signal amplitude is 5.4Vp-p.

(8) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

(9) Oscilloscope captures the signal, analyzes and processes it to obtain the measurement results.

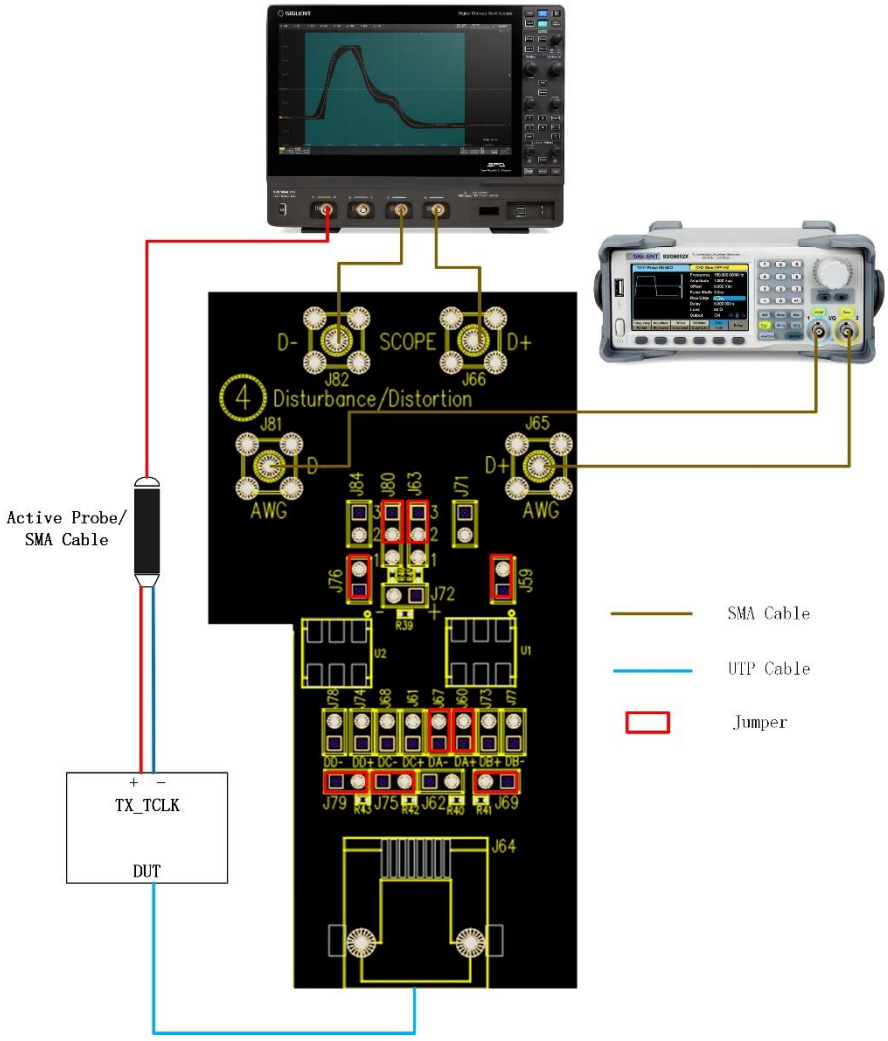


Figure 9-4 Transmitter distortion tests with TX_TCLK and with disturber

9.4.2.2 Test Procedure

(1) Configure the DUT to output test mode 4 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **With Disturber** > **Transmitter Distortion With TX_TCLK (IEEE802.3-2018, 40.6.1.2.4)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D) and average number in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal by using the same

method provided as IEEE802.3-2018, Subclause 40.6.1.2.4 in the software after acquiring the data. After finishing the tests will output the test results.

9.5 Test Results Reference

The test results of transmitter distortion tests are shown as Figure 9-5.

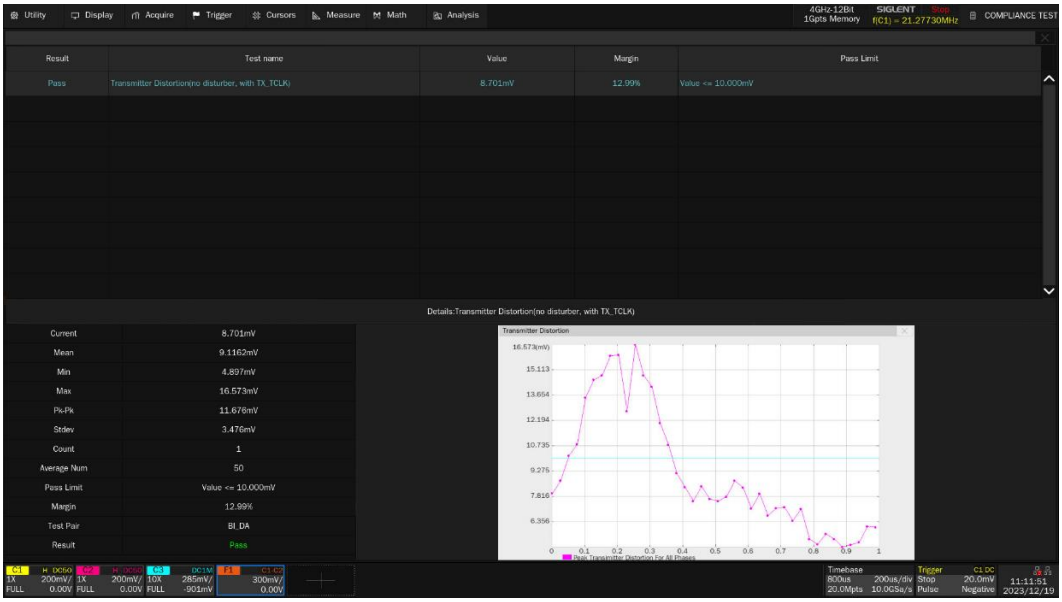


Figure 9-5 Test results of transmitter distortion tests

The details of the test waveform for transmitter distortion tests are shown as Figure 9-6.

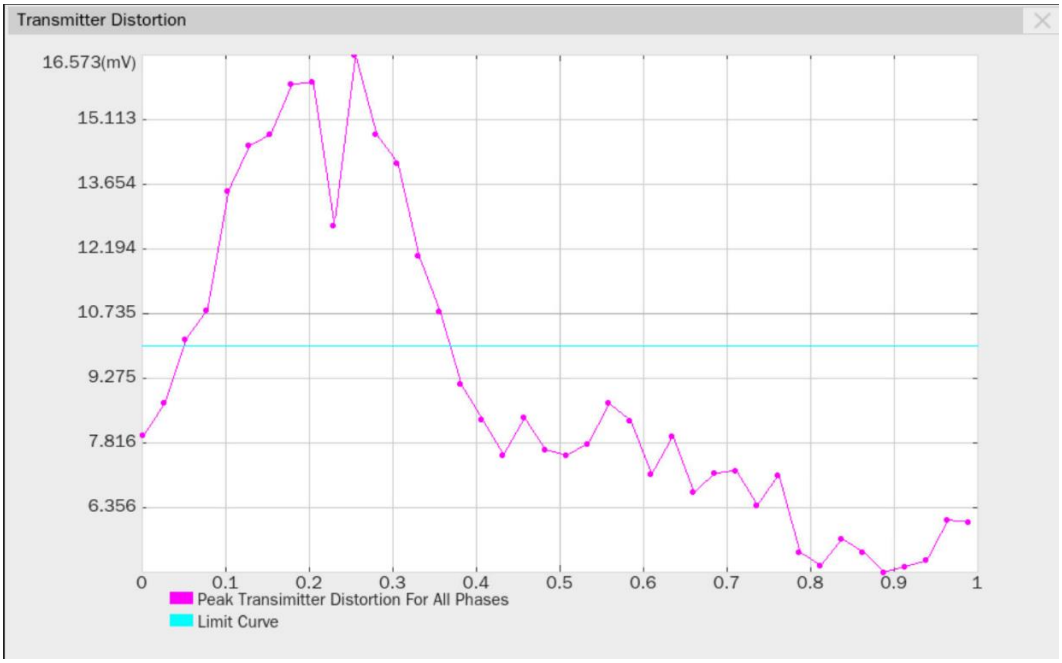


Figure 9-6 Waveform details for transmitter distortion tests

10 Jitter Tests with TX_TCLK

10.1 Test Waveform and Standard Reference

When the DUT is in test mode 2 and 3, jitter tests are used to verify whether the DUT MDI signal is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.5.

MDI output waveform is shown as Figure 10-1.

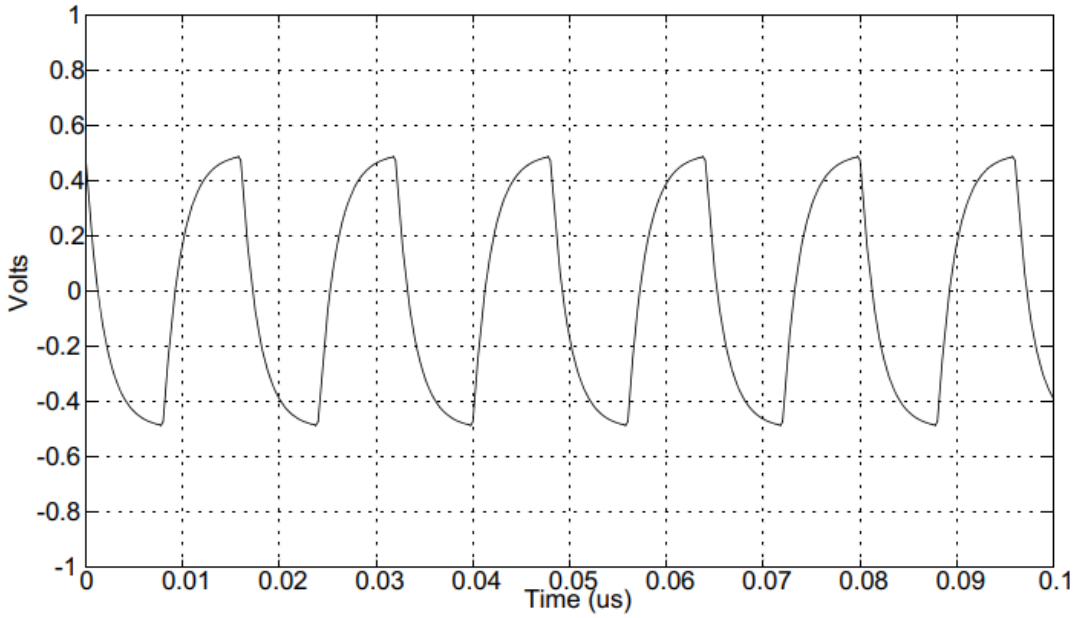


Figure 10-1 Test Mode 2 and Test Mode 3 test waveform

10.2 Jitter Tests with TX_TCLK, DUT in Master Mode

Jitter tests verifies that when the DUT is in Test Mode 2, the jitter should be within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.5.

The following jitter tests are performed for 1000 BASE-T devices with the DUT in Master mode:

- Jitter Master Mode JTXOUT: The measurements are used to verify the jitter on the MDI signal relative to the transmit clock (TX_TCLK) of the DUT. Though these measurements indirectly impact conformance, there are no specific conformance limits so the test result are reported for informative purposes.
- Jitter Master Unfiltered: While DUT in the Master timing mode, the test is used to ensure that the jitter on the DUT's transmit clock (TX_TCLK) relative to an unjittered reference is less than 1.4 ns.
- Jitter Master Filtered: The test is used to test the jitter on the DUT's transmit clock (TX_TCLK) relative to an unjittered reference after applying a 5kHz high-pass filter. The filtered DUT TX_TCLK Jitter test ensures that the filtered jitter on the DUT's transmit clock (TX_TCLK) relative to an unjittered reference plus the worst-case MASTER mode JTXOUT (over all pairs) is less than 0.3 ns

10.2.1 Jitter Master Mode JTXOUT Tests

The Master mode JTXOUT measurements are used to measure the jitter on the MDI signal relative to the transmit clock (TX_TCLK) of the DUT. Though these measurements indirectly impact conformance, there are no specific conformance limits specified. The jitter test results are reported for informative purposes.

10.2.1.1 Algorithm

When the DUT is in Test Mode 2, JTXOUT is defined as the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of the DUT transmit clock (TX_TCLK). Though these measurements indirectly impact conformance, there are no specific conformance limits specified in the IEEE802.3-2018, Subclause 40.6.1.2.5 so the test result is only for informative purpose.

However, JTXOUT is used to determine compliance when combined with filtered jitter measurements. The value of Jitter Master Mode JTXOUT is not filtered and the MDI data of the current pair and DUT transmit clock (TX_TCLK) signal should be captured between 100ms to 1 second, which contains at least 12.5 million symbol times.

The steps to analyze the jitter master mode JTXOUT is as follows:

(1) Simultaneously capture a long record with both signals (MDI data and DUT TX_TCLK).

(2) Define reference edge times as the 50% threshold crossings of the selected edge (rising or falling) of the TX_TCLK signal.

(3) Define a jitter quantity, measured from the reference edge time of TX_TCLK to the 0 V crossing of the selected edge of the MDI data signal. The jitter result for each edge on the MDI data signal is added to a jitter histogram for visualization purposes.

(4) Steps (1) to (3) are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100ms of data has been analyzed.

(5) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as JTXOUT.

(6) Record the worst JTXOUT test result among four Ethernet signal pairs (Pair A/B/C/D) as the final test result.

10.2.1.2 Test Environment and Connectivity

Jitter Master Mode JTXOUT test supports the use of SMA cables or active differential probes to probe MDI and TX_TCLK signals.

The connection with section ① on the test fixture which supports a differential active probe to probe the MDI signal, which is shown as Figure 10-2, the test step is as follows:

(1) Use a short UTP cable to connect the DUT to J28 connector on section ① of the test fixture.

(2) Use an active differential probe to probe test point (J1, J10, J21, J25) on section ① of the test fixture according to the signal pair being tested { (DA+, DA-), (DB+, DB-), (DC+,DC-), (DD+,DD-)}.

Ensure correct polarity of the probe head.

(3) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

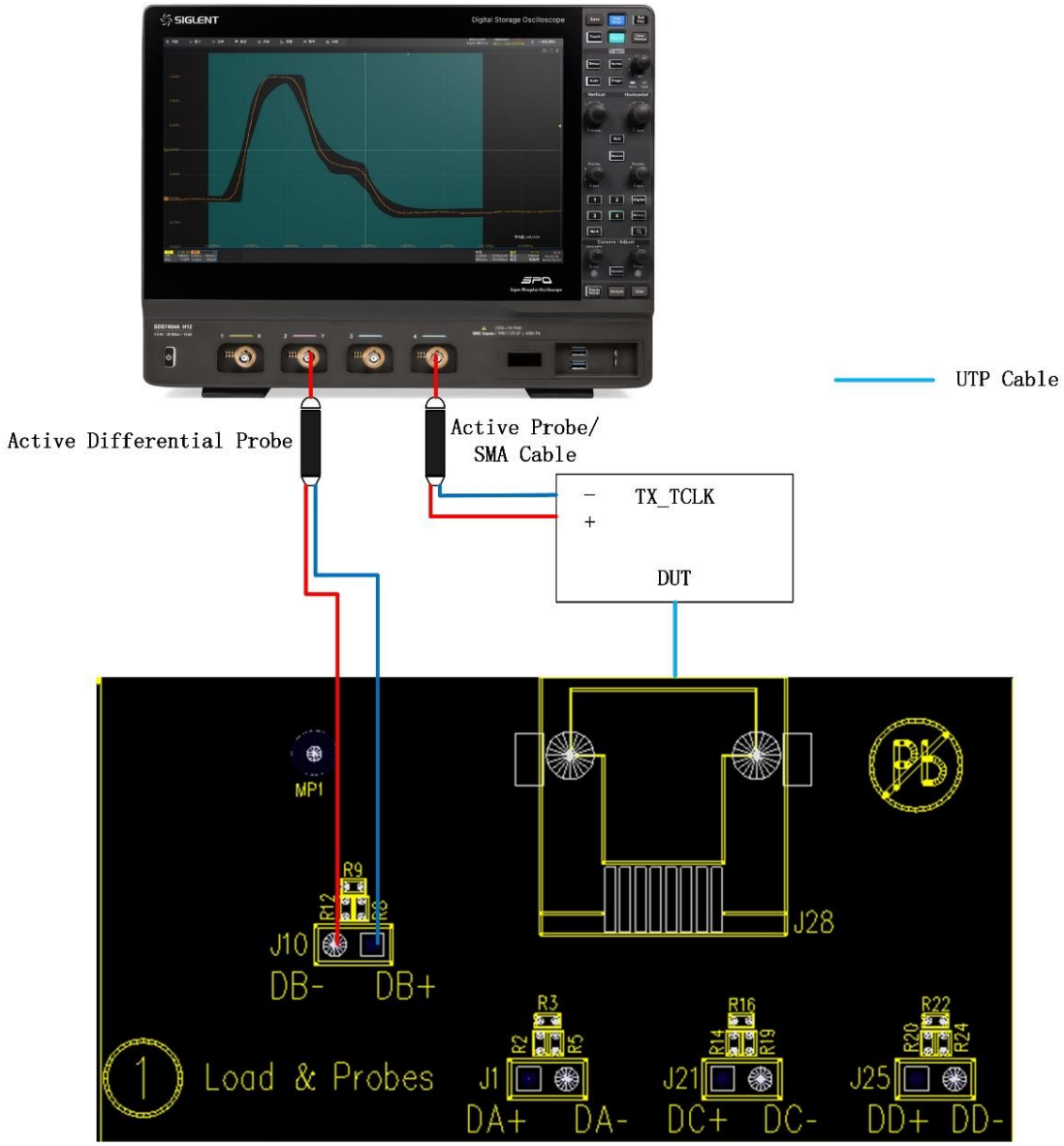


Figure 10-2 Connection of Section ① on test fixture for Master Mode JTXOUT test

The connection with section ⑥ on the test fixture which supports SMA cables to probe the MDI signal, which is shown as Figure 10-3, the test step is as follows:

(1) Use a short UTP cable to connect the DUT to the J27 connector on section ⑥ of the test fixture.

(2) According to the signal pair being tested, using two SMA cables with equal length to connect the corresponding test points {DA(J17,J4), DB(J5, J18), DC(J6, J19), DD(J7, J20)} on section ⑥ of test fixture to two input channels of the oscilloscope.

(3) Connect the other unused test points on section ⑥ of the test fixture to 50Ω terminators.

(4) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

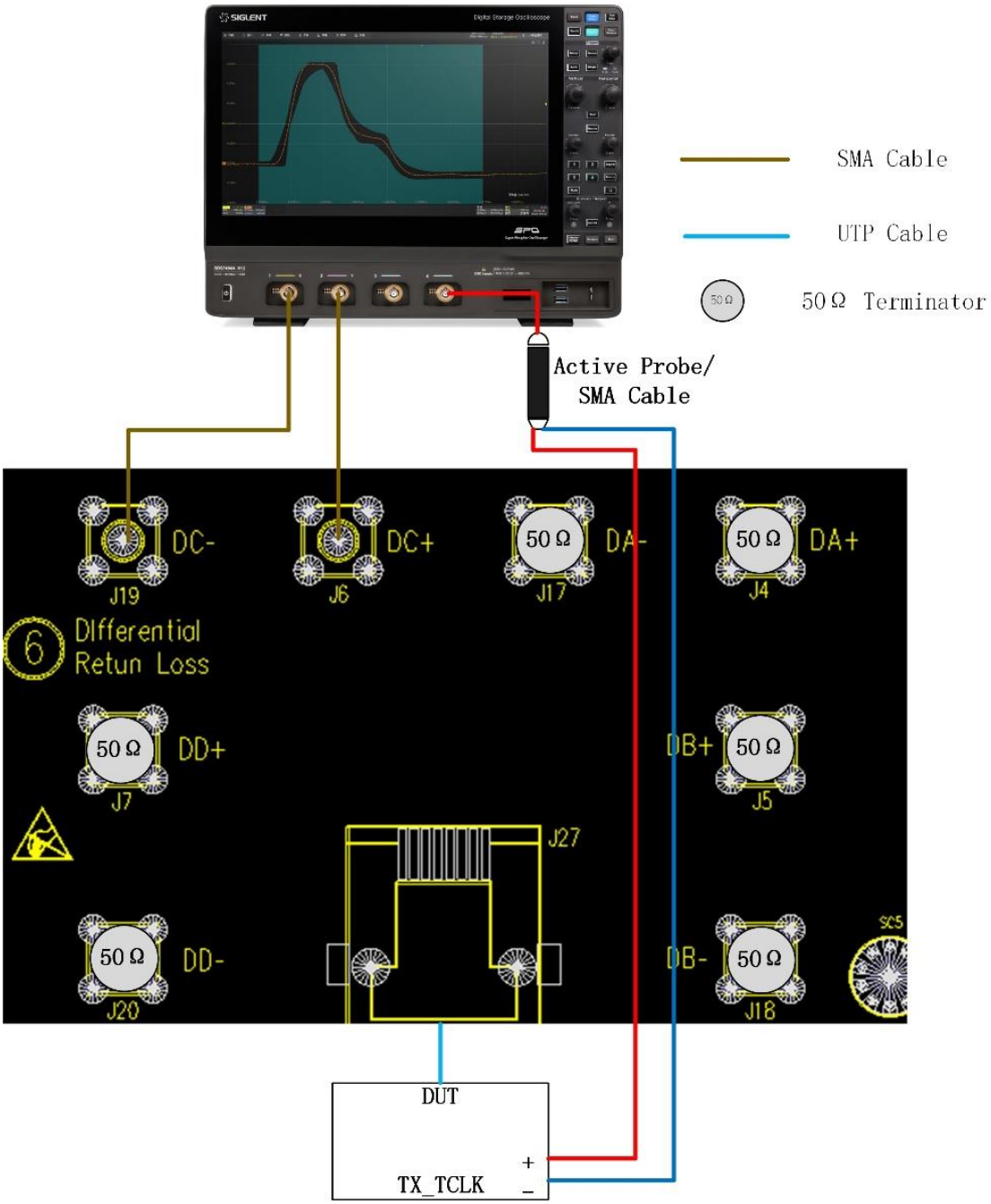


Figure 10-3 Connection of section ⑥ on test fixture for Master Mode JTXOUT test

10.2.1.3 Test Procedure

(1) Configure the DUT to output test mode 2 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Master Mode JTXOUT (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT "Source" channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal length for 100ms to 1s. After finishing the tests will output the test results.

10.2.2 Jitter Master Mode Unfiltered Tests

The test for jitter master mode unfiltered which is the test on the DUT's transmit clock (TX_TCLK) relative to an unjittered reference and the pass standard is less than 1.4 ns.

10.2.2.1 Algorithm

Set the DUT in Master Mode and test the jitter on the DUT's transmit clock (TX_TCLK) relative to an unjittered reference and the passing reference is less than 1.4 ns.

The unjittered reference is assumed to be a computed ideal clock waveform with no jitter, but actually all clocks have jitter.

In this test run, the unfiltered jitter is computed as follows:

(1) Measure all timing instants (at the 50% crossing points) of the actual clock signals over a long record.

(2) Compute the mean frequency of this measured clock signals over the entire record.

(3) The mean frequency of clock signal can be considered as an ideal unjittered reference.

(4) The jitter of each measured timing instant for the actual clock signal (DUT TX_TCLK) is computed as the deviation of the 50% crossing of the TX_TCLK from the corresponding timing instant to the computed ideal clock.

(5) The jitter value for each edge on DUT TX_TCLK signal is added to a jitter histogram.

(6) Capture 100ms to 1 second of the signals.

(7) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the Master Mode Unfiltered jitter.

10.2.2.2 Test Environment and Connectivity

The test environment is shown as Figure 10-4, the connection is shown as follows:

(1) Using a UTP cable to connect the DUT to a Link Partner.

(2) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

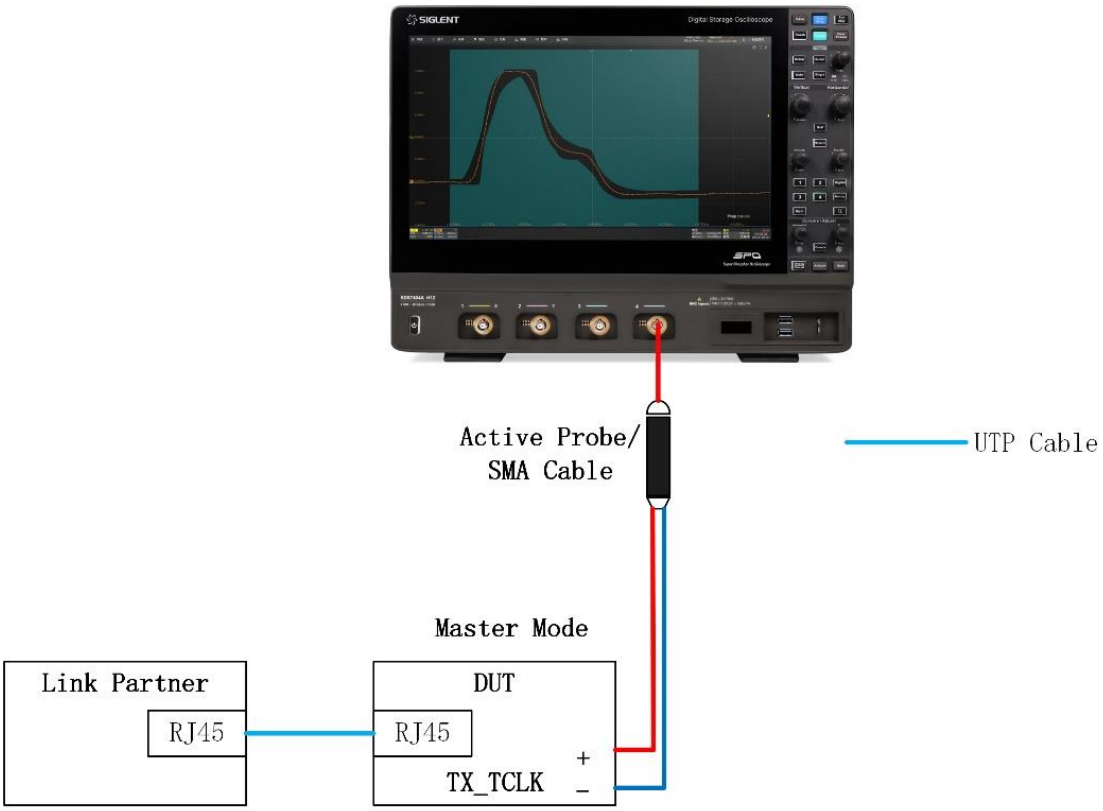


Figure 10-4 Connection for Jitter Master Mode Unfiltered by probing TX_TCLK

10.2.2.3 Test Procedure

(1) Configure the DUT to output test mode 2 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Master Mode Unfiltered (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal length from 100ms to 1s. After finishing the tests will output the test results.

Note: Configure the DUT to operate normally in the Master timing mode.

- Reset both the DUT and Link-Partner devices if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the DUT to become the MASTER.

- Ensure that the Link Partner is properly receiving data from the DUT by verifying that the Link Partner has set its GMII register bit 10.13 is set to 1.

Note: The register “bit x.y” means the address is “x” and the “y” bit in register (x and y are decima format).

10.2.3 Jitter Master Mode Filtered Tests

The test is used to test the jitter on the DUT’s transmit clock (TX_TCLK) relative to an unjittered reference after applying a 5kHz high-pass filter, the peak-to-peak value of the resulting filtered timing jitter plus JTXOUT shall be less than 0.3 ns. The DUT should be set in Master mode.

10.2.3.1 Algorithm

The algorithm proceeds as follows:

(1) Capture at least 100,000 edges of the DUT TX_TCLK signal in one long record.

(2) Compute the jitter waveform of the DUT TX_TCLK relative to an unjittered reference.

(3) Filter this jitter waveform with a 5 kHz high-pass filter to produce a filtered jitter waveform, the high-pass filter transfer function is as follows:

$$H_{jf1}(f) = \frac{jf}{jf + 5000Hz}$$

After this step of filtering, it produces a new jitter waveform.

(4) Ensure that the peak-to-peak value of the filtered jitter waveform plus the worst-case master mode JTXOUT is less than 0.3 ns.

10.2.3.2 Test Environment and Connectivity

The test environment and connection are the same as Jitter Master Mode Unfiltered, please refer to <10.2.2.2 Test Environment and Connectivity>.

10.2.3.3 Test Procedure

(1) Configure the DUT to output test mode 2 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Master Mode Filtered (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Before performing this test, ensure that the Jitter Master Mode JTXOUT was tested.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process at least 100k edges of the DUT TX_TCLK signal. After finishing the tests will output the test results.

Note: Configure the DUT to operate normally in the Master timing mode.

- Reset both the DUT and Link-Partner devices if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the DUT to become the MASTER.
- Ensure that the Link Partner is properly receiving data from the DUT by verifying that the Link Partner has set its GMII register bit 10.13 is set to 1.

Note: The register “bit x.y” means the address is “x” and the “y” bit in register (x and y are decima format).

10.2.4 Test Results Reference

The test result reference for Jitter with TX_TCLK when DUT is in master mode is shown as Figure 10-5. The waveform details for Jitter Master Mode JTXOUT are shown as Figure 10-6.

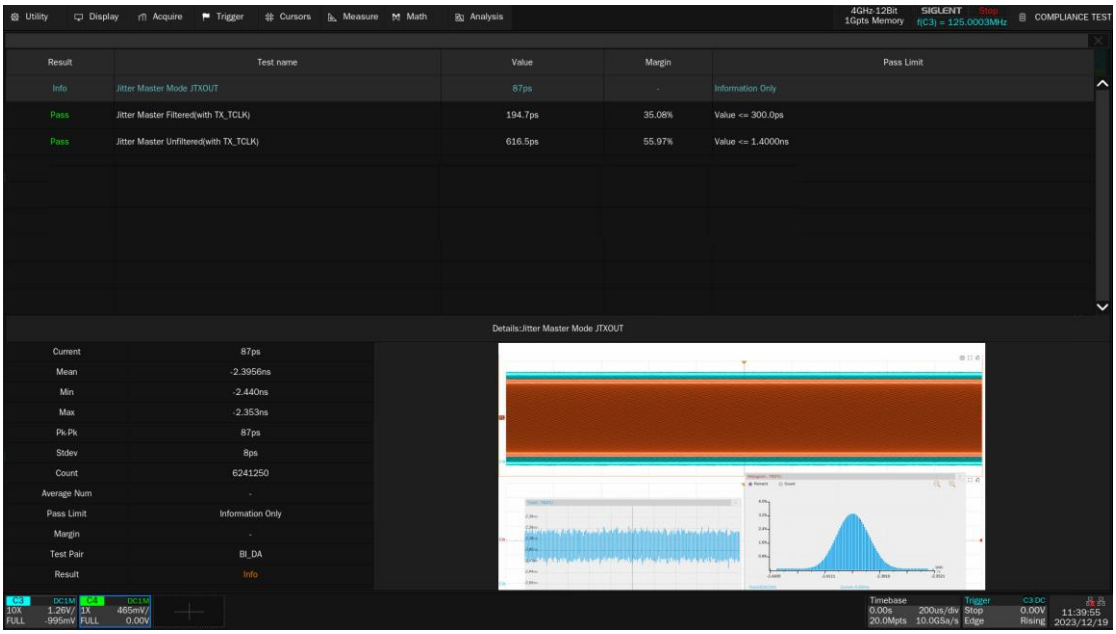


Figure 10-5 Reference results for jitter tests with TX_TCLK when DUT in master mode

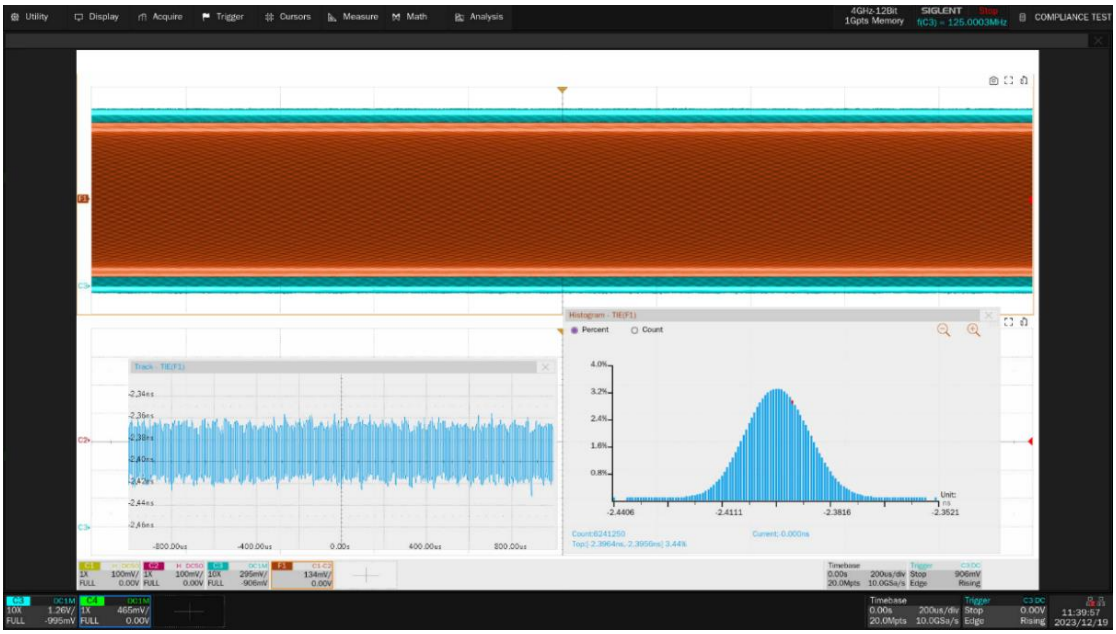


Figure 10-6 Waveform details for JTXOUT when DUT in master mode

10.3 Jitter Tests with TX_TCLK, DUT in Slave Mode

These tests verify that the jitter of DUT (DUT in slave mode) is within the specified range in IEEE802.3-2018, Subclause 40.6.1.2.5.

Jitter tests with TX_TCLK when DUT is in slave mode needs to test the following items:

- Jitter Slave Mode JTXOUT: Measures the jitter on the MDI data relative to the DUT transmit clock (TX_TCLK) while DUT in SLAVE timing mode. Though these measurements indirectly impact conformance, there are no specific conformance limits. The results are reported for informative purposes.
- Jitter Slave Mode Unfiltered: Measures the unfiltered jitter on the DUT transmit clock (TX_TCLK) signal relative to a link-partner's Master transmit clock (TX_TCLK). This test is performed while the DUT is operating normally as the Slave. Connected DUT to a link partner with the Test Channel, and the Test Channel is recommended by the IEEE802.3-2018, Subclause 40.6.1.1.1 in the Test Channel chapter. The test run captures and processes 100ms to 1 second signal for the peak-to-peak jitter without filtering and ensures the value is less than 1.4ns.
- Jitter Slave Mode filtered: The test captures at least 100k edges of the DUT TX_TCLK and the Link Partner TX_TCLK signals and measures the same jitter quantity (DUT Slave TX_TCLK relative to Master TX_TCLK) after filtering the jitter waveform with a 32 kHz high-pass filter. This test also simultaneously measures the jitter on the Master TX_TCLK relative to an unjittered reference after filtering this jitter waveform with a 5 kHz high-pass filter. This test also uses the worst Slave JTXOUT measurement to determine compliance. The results of filtered peak-to-peak jitter for DUT (Slave) plus the worst DUT JTXOUT minus the jitter of Link Partner (Master) TX_TCLK filtered by 5kHz high-pass filter must less than 0.4ns.

10.3.1 Jitter Slave Mode JTXOUT Tests

Jitter salve mode JTXOUT is defined as the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of the DUT transmit clock (TX_TCLK). The results are reported for informative purpose.

10.3.1.1 Algorithm

When the DUT is in slave timing (Test Mode 3), JTXOUT is defined as the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of the DUT transmit clock (TX_TCLK). Though these measurements indirectly impact conformance, there are no specific conformance limits specified in the IEEE802.3-2018, Subclause 40.6.1.2.5 so the test result only for informative purpose.

However, JTXOUT is used to determine compliance when combined with filtered jitter measurements. The value of Jitter Slave Mode JTXOUT is not filtered, and the MDI data of the current pair and DUT transmit clock (TX_TCLK) signal should be captured between 100ms to 1 second, which contains at least 12.5 million symbol times.

The steps to analyze the Slave mode JTXOUT is as follows:

(1) Simultaneously capture a long record with both signals (MDI data and DUT TX_TCLK).

(2) Define reference edge times as the 50% threshold crossings of the selected edge (rising or falling) of the TX_TCLK signal.

(3) Define a jitter quantity, measured from the reference edge time of TX_TCLK to the 0 V crossing of the selected edge of the MDI data signal. The jitter result for each edge on the MDI data signal is added to a jitter histogram for visualization purposes.

(4) Steps (1) to (3) are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100ms of data has been analyzed.

(5) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as JTXOUT.

(6) Record the worst JTXOUT test result among four Ethernet signal pairs (Pair A/B/C/D) as the final test result.

10.3.1.2 Test Environment and Connectivity

Jitter Slave Mode JTXOUT test supports the use of SMA cables or active differential probes to probe MDI and TX_TCLK signals.

The connection with section ① on the test fixture which supports a differential active probe to probe the MDI signal, which is shown as Figure 10-7, the test step is as follows:

(1) Use a short UTP cable to connect the DUT to J28 connector on section ① of the test fixture.

(2) Use an active differential probe to probe test point (J1, J10, J21, J25) on section ① of the test fixture according to the signal pair being tested { (DA+, DA-), (DB+, DB-), (DC+,DC-), (DD+,DD-)}. Ensure correct polarity of the probe head.

(3) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

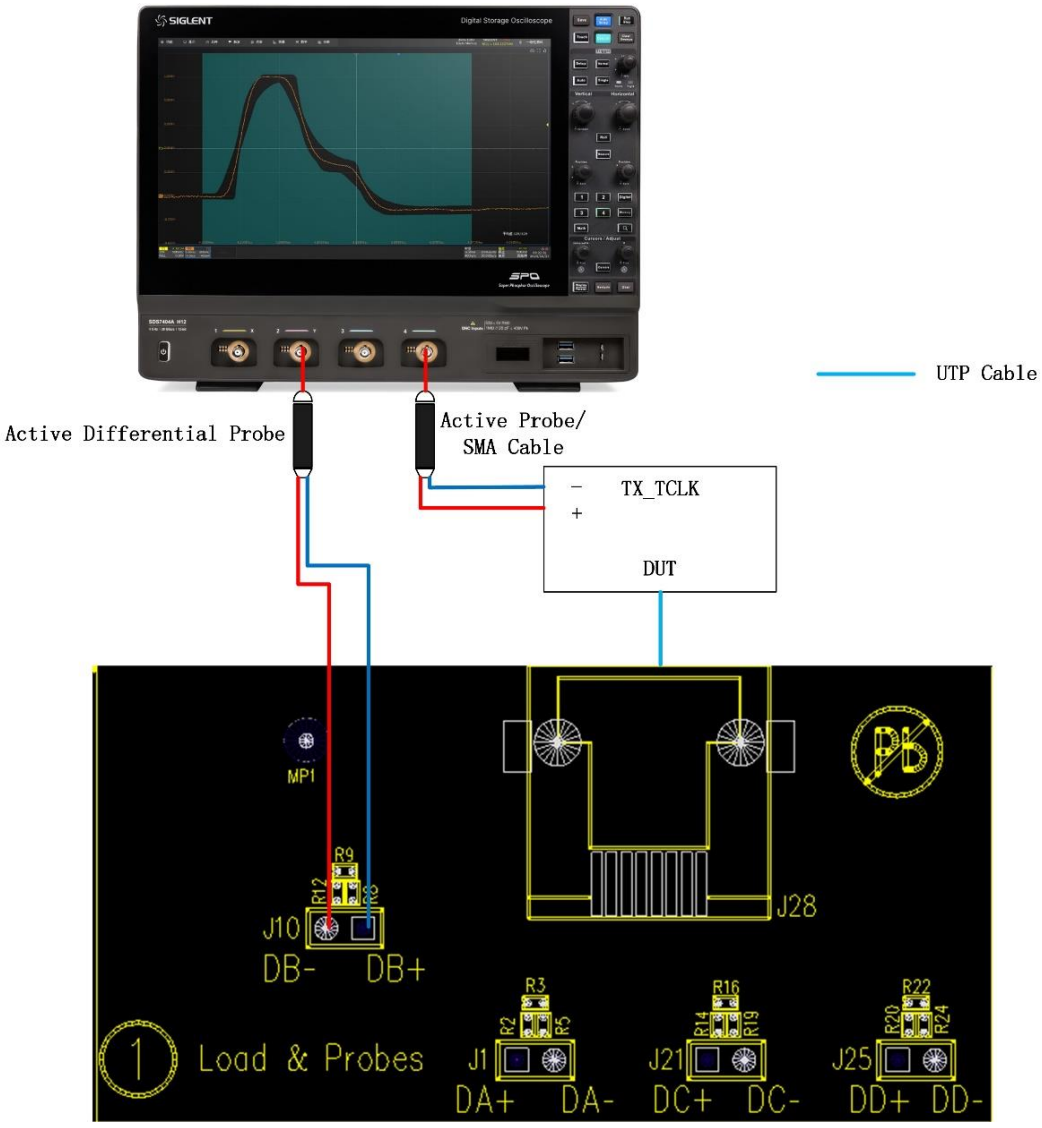


Figure 10-7 Connection of Section ① on test fixture for Slave Mode JTXOUT test

The connection with section ⑥ on the test fixture which supports SMA cables to probe the MDI signal, which is shown as Figure 10-8, the test step is as follows:

(1) Use a short UTP cable to connect the DUT to the J27 connector on section ⑥ of the test fixture.

(2) According to the signal pair being tested, using two SMA cables with equal length to connect the corresponding test points {DA(J17,J4), DB(J5, J18), DC(J6, J19), DD(J7, J20)} on section ⑥ of test fixture to two input channels of the oscilloscope.

(3) Connect the other unused test points on section ⑥ of the test fixture to 50Ω terminators.

(4) Connect the DUT's TX_TCLK to one input channel of the oscilloscope by using an active probe or a SMA cable.

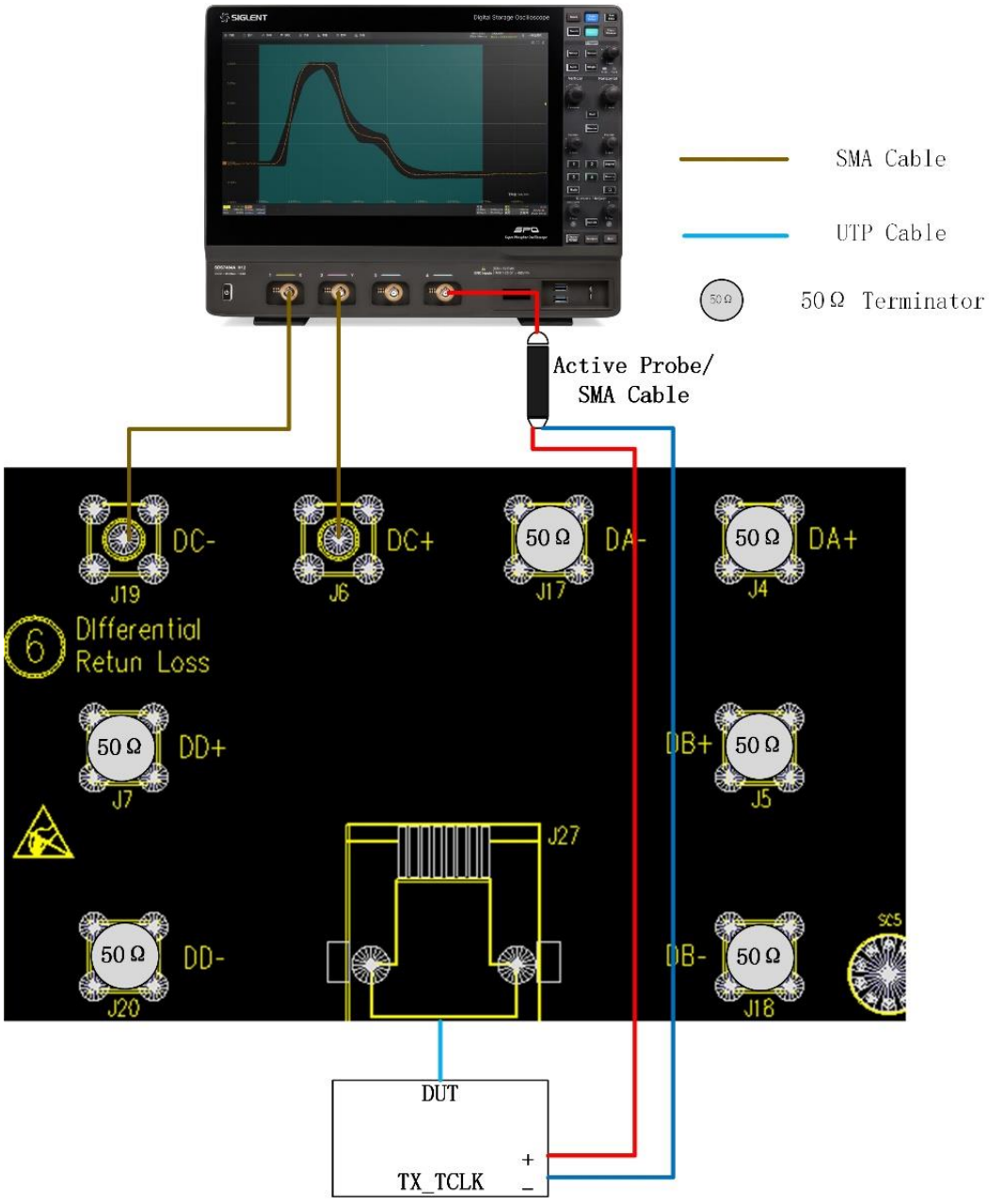


Figure 10-8 Connection of Section ⑥ on test fixture for Slave Mode JTXOUT test

10.3.1.3 Test Procedure

(1) Configure the DUT to output test mode 3 signal (Slave timing mode).

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Slave Mode JTXOUT (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the

Connect step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal length for 100ms to 1s. After finishing the tests will output the test results.

10.3.2 Jitter Slave Mode Unfiltered Tests

Jitter Slave Mode Unfiltered is the test by measuring the unfiltered jitter on the DUT transmit clock (TX_TCLK) signal relative to a link-partner’s Master transmit clock (TX_TCLK). This test is performed while the DUT is operating normally as the Slave, connected to a link partner operating as the Master, the connection is via the Test Channel. The jitter should be less than 1.4 ns to pass the conformance test.

10.3.2.1 Algorithm

This section discusses algorithms for measuring unfiltered Slave mode TX_TCLK jitter of the DUT. This test is carried out while the DUT is operating in Slave timing mode, connected to a link partner operating in Master timing mode with the jitter test channel. The test measures the peak-to-peak jitter on the DUT’s transmit clock (TX_TCLK) relative to the Master transmit clock (TX_TCLK). This is a two-clock jitter measurement.

Define ideal reference edges as the 50% threshold crossings of the Master (link partner) TX_TCLK signal.

Measure each rising edge of DUT TX_TCLK signal, as the time difference between the 50% crossing of the TX_TCLK signal to the time of its corresponding ideal reference edge. The jitter result for each rising edge on DUT TX_TCLK signal is added to a jitter histogram.

Analyze 100ms to 1 second of the data. This corresponds to at least 12.5 million clock periods.

The peak-to-peak value over the entire jitter population is recorded as Jitter Slave Mode Unfiltered with TX_TCLK and ensure that the value is less than 1.4ns to pass the conformance test.

10.3.2.2 Test Environment and Connectivity

In the formal test, the connectivity of this test is quite complex. So, in normal test, use a general 103m long ethernet cable instead to directly connect Link Partner (Master) and DUT (Slave), and after the DUT recovers the Link Partner's clock, test the jitter of TX_TCLK on the DUT relative to the TX_TCLK on the Link Partner.

In the formal test for Jitter Slave Mode Unfiltered with TX_TCLK, a special cable is required as recommended by the standard reference IEEE802.3-2018 in the <Subclause 40.6.1.1.1 Test channel> section, the test cable can be manufactured as shown in Figure 10-9, with port A on the cable connected close to the DUT.

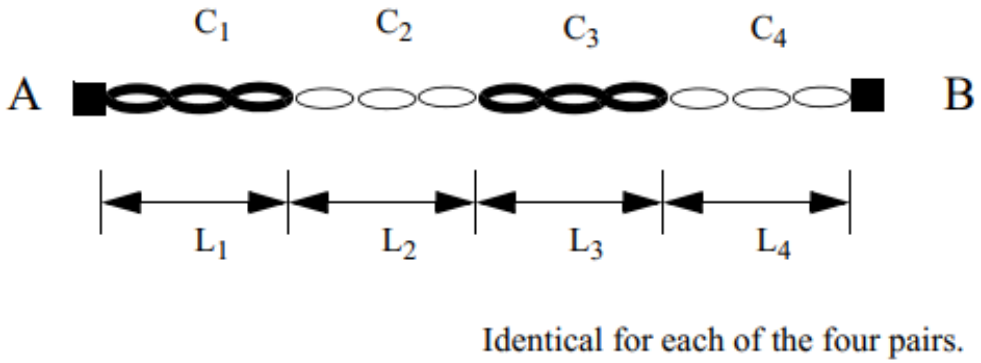


Figure 40–19—Test channel topology for each cable pair

Table 40–6—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	L_1=1.20	120 Ω ± 5 Ω	7.8 to 8.8 dB
2	L_2=x	100 Ω ± 5 Ω	10.8 to 11.8 dB
3	L_3=1.48	120 Ω ± 5 Ω	7.8 to 8.8 dB
4	L_4=y	100 Ω ± 5 Ω	10.8 to 11.8 dB

Figure 10-9 Test channel specification in IEEE802.3 standard for connecting DUT to Link Partner

The test channel as defined in Figure 10-9 can be applied to the test environment as Figure 10-10 shown. The test channel is used to connect the Link Partner (Master) to the J30 connector on the section ⑦ on the text fixture. The test environment is set up as follows:

(1) Connect the DUT (work in Slave mode) to the J29 connector on section ⑦ of the test fixture by using a short UTP cable.

(2) Connect the Link Partner (work in Master mode) to the J30 connector on section ⑦ of the test fixture by using a long UTP cable (Test spool).The Test Spool is made according to the test channel specification as defined in Figure 10-9.

(3) Connect the TX_TCLK of Link Partner to one input channel of the oscilloscope by using an active probe or a SMA cable.

(4) Connect the TX_TCLK of DUT to another input channel of the oscilloscope by using an active probe or a SMA cable.

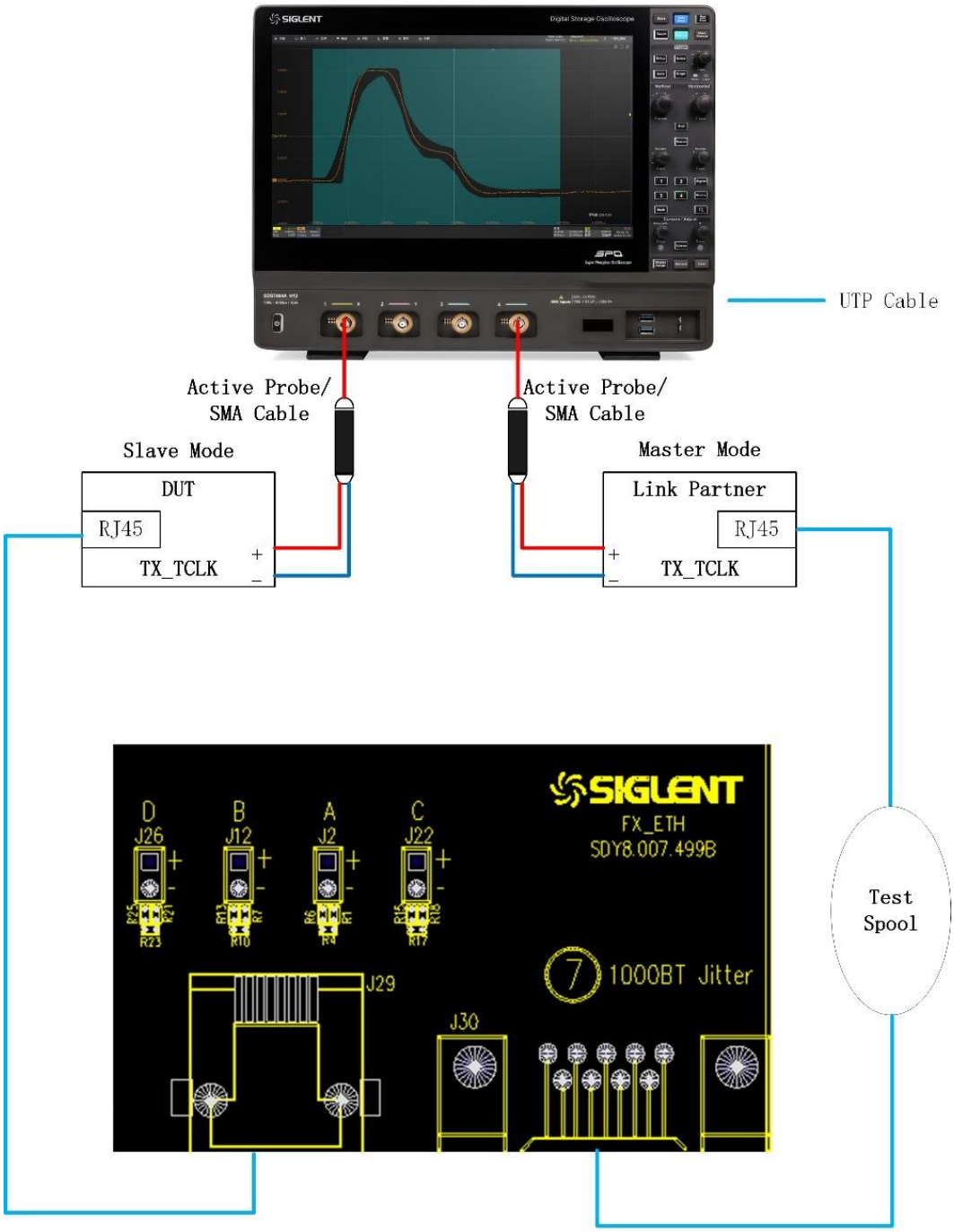


Figure 10-10 Probing for 1000 BASE-T Slave TX_TCLK Jitter (Filtered and Unfiltered)

10.3.2.3 Test Procedure

(1) Configure the Link Partner operating as the Master and DUT operating normally in the Slave timing.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Slave Mode Unfiltered (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test**.

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT "Source" channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal length from 100ms to 1s. After finishing the tests will output the test results.

Note: Configure the Link Partner to operate normally in the Master timing mode. Ensure that a valid link exists between the DUT and the Link Partner.

- Reset the Link-Partner device if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the Link Partner to become the Master.

Note: Configure the DUT to operate normally in the Slave timing mode.

- Reset the DUT device if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the DUT to become the SLAVE.
- Ensure that the DUT is properly receiving data from the Link Partner by verifying that the DUT has set its GMII register bit 10.13 is set to 1.

Note: Ensure that both TX_TCLK signals (DUT and Link-Partner) are being captured and that their phase relationship is relatively stable over multiple acquisitions. This indicates that the Slave clock is tracking the Master.

Note: The register "bit x.y" means the address is "x" and the "y" bit in register (x and y are decima format).

10.3.3 Jitter Slave Mode Filtered Tests

With the DUT operating in the Slave timing mode and a Link-Partner operating in the Master timing mode, the filtered DUT TX_TCLK captures at least 100,000 edges of the DUT TX_TCLK and the Link Partner TX_TCLK signals. And measures the same jitter quantity (DUT Slave TX_TCLK relative to Master TX_TCLK) then filtering the jitter with a 32 kHz high-pass filter. This test also simultaneously measures the jitter on the Master TX_TCLK relative to an unjittered reference then filtering this jitter with a 5 kHz high-pass filter. This test also uses the worst Slave JTXOUT measurement to determine compliance. The results of peak-to-peak jitter in Slave mode plus the worst Slave JTXOUT minus the jitter of Link Partner (Master) TX_TCLK filtered by 5kHz high-pass filter must be less than 0.4ns.

10.3.3.1 Algorithm

The filtered DUT TX_TCLK test measurement is: Measure the filtered jitter on the Master (link partner) TX_TCLK itself relative to an unjittered reference, then filtering this jitter with a 5 kHz high-pass filter to get the peak-to peak jitter value.

And measures the same jitter quantity (DUT Slave TX_TCLK relative to Master TX_TCLK) then filtering the jitter with a 32 kHz high-pass filter.

Section <10.3.2.1 Algorithm> discusses the computation of an unfiltered jitter waveform of the Slave (DUT) TX_TCLK relative to the Master (link partner) TX_TCLK signal. Capture the DUT TX_TCLK and the Link Partner TX_TCLK signals and compute a jitter and filter this jitter waveform with a 32kHz high-pass filter to produce a filtered jitter waveform.

The transfer function for 32kHz high-pass filter is as follows:

$$H_{jf2}(f) = \frac{jf}{jf + 32000Hz}$$

The method to compute TX_TCLK jitter of Link Partner (Master), please refer to chapter <10.2.2.1 Algorithm> and <10.2.3.1 Algorithm>.

The steps to analyze the filtered jitter for DUT (Slave mode) with TX_TCLK is as follows:

(1) Simultaneously capture a long record of at least 100,000 edges of the DUT TX_TCLK and the link partner TX_TCLK signals.

(2) Define reference edges for the jitter measurement as the 50% threshold crossing times of the Master (link-partner) TX_TCLK signal.

(3) Define a jitter quantity, measured for each rising edge of DUT TX_TCLK signal, as the time difference between the 50% crossing of the TX_TCLK signal to the time of its corresponding reference edge.

(4) Compute a jitter waveform of the simultaneously captured Master (link partner) TX_TCLK signal relative to an unjittered reference and filter this jitter waveform with a 5kHz high-pass and then compute the jitter.

(5) Ensure the results of DUT peak-to-peak jitter filtered by 32kHz high-pass filter plus the worst Slave JTXOUT minus the jitter of Link Partner (Master) TX_TCLK filtered by 5kHz high-pass filter must less than 0.4ns.

10.3.3.2 Test Environment and Connectivity

The test environment is the same as <10.3.2.2 Test Environment and Connectivity>.

10.3.3.3 Test Procedure

(1) Configure the Link Partner operating as the Master and DUT operating normally in the Slave timing.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter With TX_TCLK** > **Jitter Slave Mode filtered（IEEE802.3-2018, 40.6.1.2.5）** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal for at least 100k edges. After finishing the tests will output the test results.

Note: Configure the Link Partner to operate normally in the Master timing mode. Ensure that a valid link exists between the DUT and the Link Partner.

- Reset the Link-Partner device if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the Link Partner to become the Master.

Note: Configure the DUT to operate normally in the Slave timing mode.

- Reset the DUT device if necessary.
- Set bit 9.12 to enable MASTER-SLAVE Manual Configuration.
- Set bit 9.11 to force the DUT to become the SLAVE.
- Ensure that the DUT is properly receiving data from the Link Partner by verifying that the DUT has set its GMII register bit 10.13 is set to 1.

Note: Ensure that both TX_TCLK signals (DUT and Link-Partner) are being captured and that their phase relationship is relatively stable over multiple acquisitions. This indicates that the SLAVE clock is tracking the Master.

Note: The register “bit x.y” means the address is “x” and the “y” bit in register (x and y are decima format).

10.3.4 Test Results Reference

The reference result of Jitter Slave Mode with TX_TCLK is shown as Figure 10-11. The waveform details are shown as Figure 10-12.

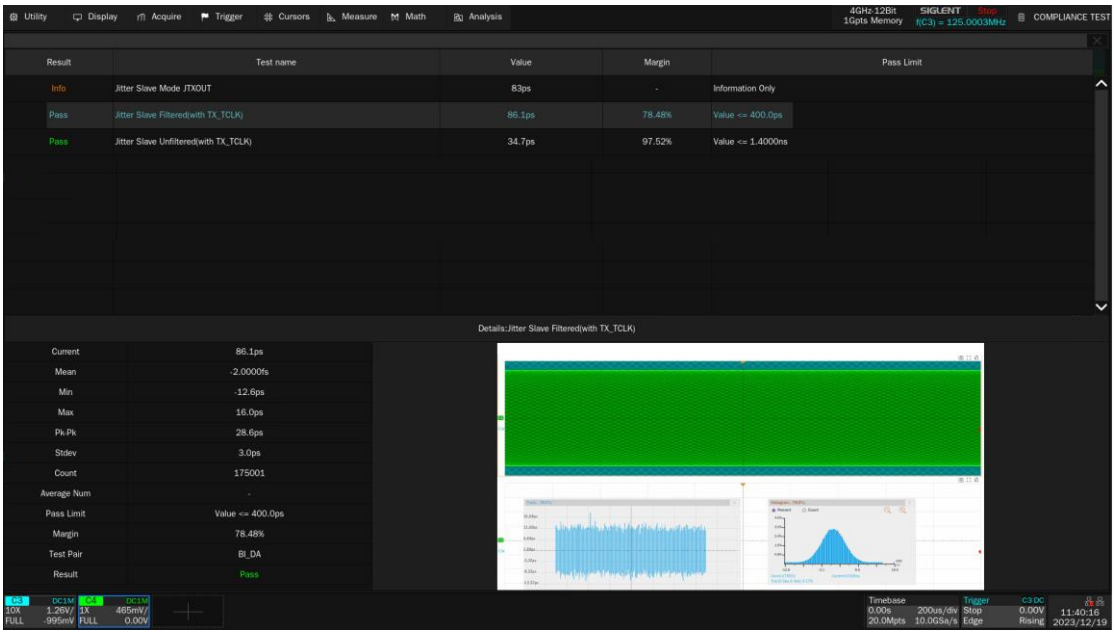


Figure 10-11 Reference results of Jitter Slave Mode with TX_TCLK

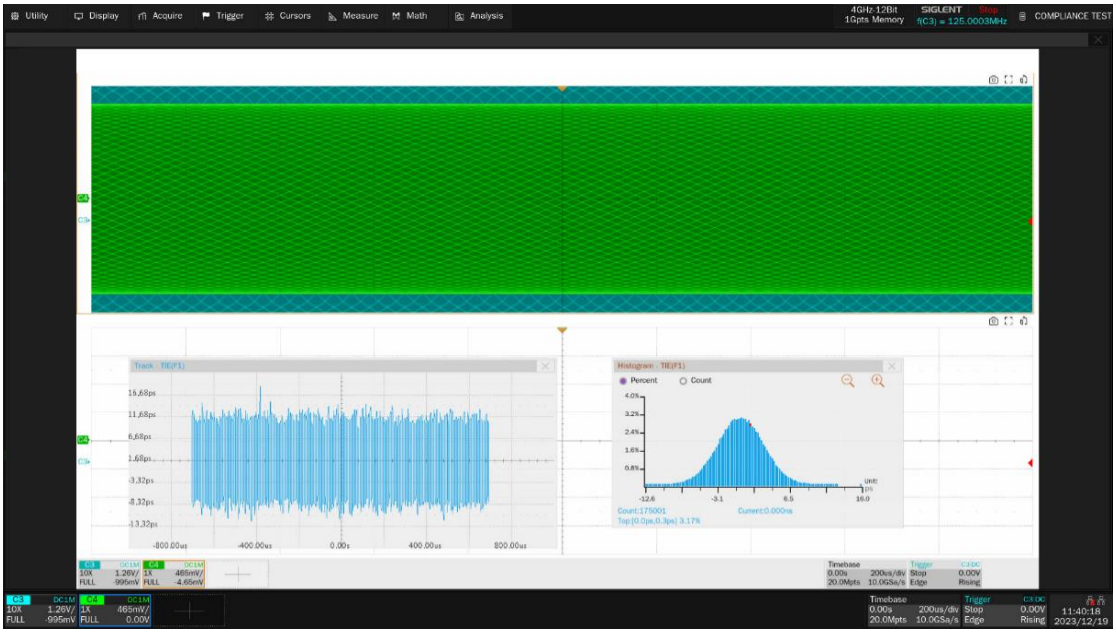


Figure 10-12 Waveform details of Jitter Slave Mode Filtered with TX_TCLK

11 Jitter Tests Without TX_TCLK

Not all DUT provide access to TX_TCLK. Hence, in the case where your DUT does not provide access to TX_TCLK, it might be possible to perform an alternative and simpler version of the full jitter test procedure which could compute the Jitter in Master and Slave mode without TX_TCLK, and provide some helpful information for the tests under this section.

Note: This is an alternate test method for jitter measurement being proposed, when TX_TCLK is not accessible. This is an informal test method.

If you want to intensive study the jitter tests without TX_TCLK, you can read the chapter “Appendix 40.B – Transmitter Timing Jitter, No TX_TCLK access”, which is part of the technical document “Gigabit Ethernet Consortium Clause 40 PMA Test Suite, version 2.6”. The Gigabit Ethernet Consortium is based at the University of New Hampshire Interoperability Lab.

11.1 Jitter Tests Without TX_TCLK, DUT in Master Mode

According to IEEE802.3-2018, Subclause 40.6.1.2.5, JTXOUT has to be measured before running the filtered jitter test as the result of the filtered jitter test is the summation of the filtered TX_TCLK jitter plus the unfiltered JTXOUT. This test does not require the JTXOUT measurement for the reason that it should assume JTXOUT is small compared to the filtered TX_TCLK jitter in actual systems.

Jitter tests without TX_TCLK when DUT is in Master Mode can be divided in:

- Jitter MASTER Unfiltered: Computes the unfiltered jitter on the Master output at the MDI relative to an unjittered reference while in the Master timing mode.
- Jitter MASTER Filtered: Computes the unfiltered jitter on the Master output at the MDI relative to an unjittered reference while in the Master timing mode and filtered by a 5kHz high-pass filter.

11.1.1 Jitter Master Mode Unfiltered Tests

Configure the DUT to output the Test Mode 2 signal (Master) and compute the jitter on the Master output MDI relative to the unjittered reference, ensure that the jitter is less than 1.4ns. This test will be inconclusive if the peak-to-peak result is greater than 1.4ns.

11.1.1.1 Algorithm

Since the DUT doesn’t provide access to TX_TCLK and the Master jitter at MDI is assumed to be identical to the jitter on the internal TX_TCLK, it is reasonable to measure the peak-to-peak jitter at MDI.

According to IEEE802.3-2018, Subclause 40.6.1.2.5, the DUT unfiltered jitter of TX_TCLK should be less than 1.4ns. This test will be inconclusive if the result is greater than 1.4ns.

The unfiltered jitter measurements shall be made in between 100ms and 1 second. This corresponds to at least 12.5 million clock periods. The steps to analyze the jitter is as follows:

(1) Capture a long record of the signal at MDI.
(2) Compute ideal clock according to the method discussed in <10.2.2.1 Algorithm>.
(3) Define a jitter quantity for each measured timing instant of the signal at MDI as the deviation of the 50% crossing of the signal to its corresponding ideal clock edge.
(4) The jitter value for each edge on the signal at MDI is added to a jitter histogram for visualization purposes.
(5) Steps (1) to (4) are repeated to acquire new data and accumulate the jitter histogram with each new acquisition until at least 100ms of data has been analyzed.
(6) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the unfiltered Master without TX_TCLK jitter.
(7) The test is pass when jitter is less than 1.4ns. The test will be inconclusive if the peak-to-peak result is greater than 1.4ns.

11.1.1.2 Test Environment and Connectivity

Test environment and connection for jitter tests without TX_TCLK when DUT is in master mode, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

11.1.1.3 Test Procedure

(1) Configure the DUT to output Test Mode 2 signal.
(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter Without TX_TCLK** > **Jitter Master Mode Unfiltered（IEEE802.3-2018, 40.6.1.2.5）** .
(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.
(4) Check the correctness of the test environment setup in the **Connect** tab.
(5) Click **Run Test** .
(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal between 100ms to 1 second length signal. After finishing the tests will output the test results.

11.1.2 Jitter Master Mode Filtered Tests

Configure the DUT to output the Test Mode 2 signal (Master timing) and compute the jitter on the MDI output relative to the unjittered reference then applying a 5kHz high-pass filter, the tests fails if the filtered jitter result is greater than 0.3ns. This test will be inconclusive if the peak-to-peak jitter is less than 0.3ns.

11.1.2.1 Algorithm

In IEEE802.3-2018, Subclause 40.6.1.2.5, the unfiltered JTXOUT (it is the jitter between DUT TX_TCLK and the MDI data signal) is added into the filtered Master jitter test. Hence, the test without TX_TCLK should be easier to pass. If the DUT produces a value greater than 0.3ns, we can say that the test has failed.

Remember that the results obtained using this approach are inconclusive when the peak-to-peak jitter is less than 0.3 ns because it is not possible to know how much of this value is contributed by JTXOUT, unlike the formal test which measures the JTXOUT prior being added to the filtered TX_TCLK Master Mode jitter that is exposed to TX_TCLK.

The measurement for this test is separated into two parts. The first part is to compute the jitter waveform of the MDI data signal relative to an unjittered reference which is the same as mentioned in Jitter Master Unfiltered without TX_TCLK. Then, filter the unfiltered jitter waveform with a 5 kHz high-pass filter and get the result of peak-to-peak jitter.

Jitter Master Mode Filtered Test need to measure at least 100,000 clock edges and the algorithm proceeds as follows:

(1) Capture at least 100,000 edges of the signal at MDI.

(2) Compute the jitter waveform of the signal at MDI relative to an unjittered reference and filter this jitter waveform with a 5kHz high-pass filter to produce a filtered jitter waveform.

(3) The jitter value for each edge on the signal at MDI is added to a jitter histogram for visualization purposes.

(4) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the filtered master jitter without TX_TCLK.

(5) The tests fails if the filtered jitter result is greater than 0.3ns. The test will be inconclusive if the peak-to-peak jitter is less than 0.3ns.

11.1.2.2 Test Environment and Connectivity

Test environment and connection for jitter tests without TX_TCLK when DUT is in master mode, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

11.1.2.3 Test Procedure

(1) Configure the DUT to output Test Mode 2 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter Without TX_TCLK** > **Jitter Master Mode Filtered (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the

Connect step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal for at least 100,000 edges. After finishing the tests will output the test results.

11.1.3 Test Results Reference

The reference result of Jitter Master Mode Without TX_TCLK is shown as Figure 11-1. The waveform details are shown as Figure 11-2.

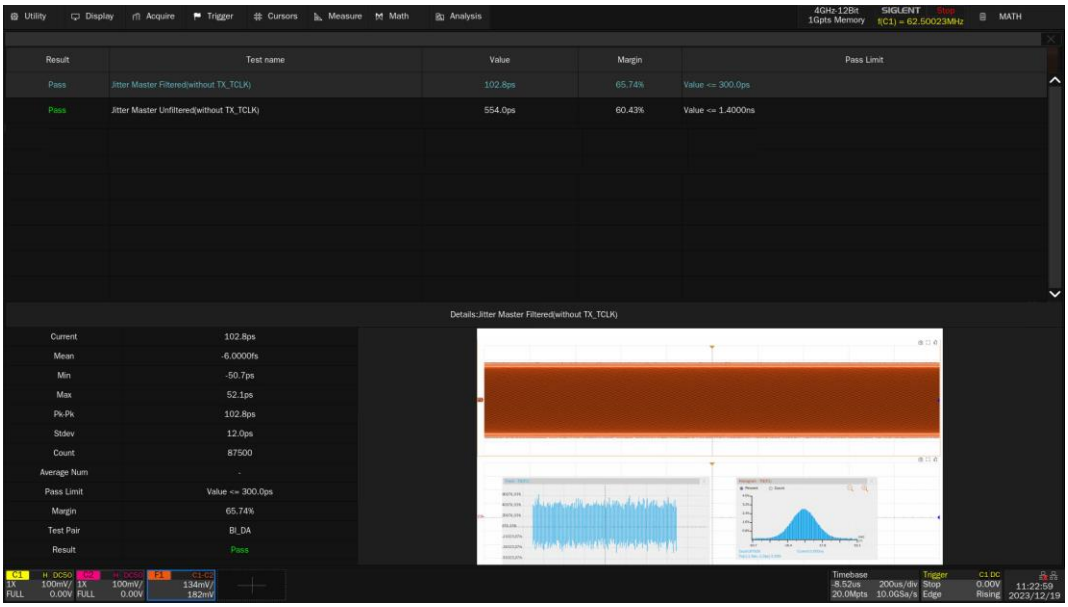


Figure 11-1 Reference results of Jitter Master Mode Without TX_TCLK

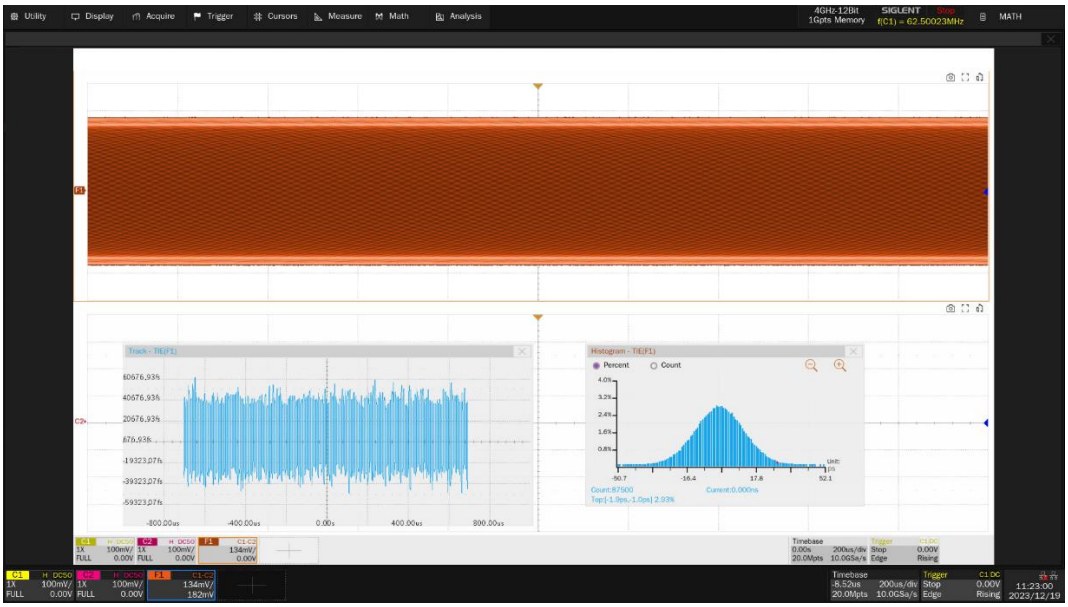


Figure 11-2 Waveform details of Jitter Master Mode Filtered Without TX_TCLK

11.2 Jitter Tests Without TX_TCLK, DUT in Slave Mode

In the formal procedure for Jitter Slave Mode Test as <10.3 Jitter Tests with TX_TCLK, DUT in Slave Mode>shown, which needs both Master (Link partner) and Slave (DUT) to provide two TX_TCLK signals to support the test which makes the test complex. Apart from that, a Slave DUT needs a PHY to provide a signal at the MDI and uses it to recover the TX_TCLK which is not possible to measure the jitter at the SLAVE's MDI output due to the fact that each MDI wire pair is bi-directional.

Thus, the test in this chapter can be supported by configuring the DUT to test mode 3 to simplify the test environment.

Before starting the test, make sure you have already run the Master jitter test on the signal pair that you want to measure, which are Jitter Master Mode Unfiltered and Filtered without TX_TCLK, the peak-to-peak values are needed for the following tests.

Jitter Slave Mode without TX_TCLK is divided in:

- Jitter Slave Unfiltered: Compute the unfiltered jitter on the Slave output at MDI relative to an unjittered reference and record as unfiltered Slave. Subtract unfiltered Slave jitter with unfiltered Master jitter without TX_TCLK jitter.
- Jitter Slave Filtered: Compute the jitter on the Slave output at MDI relative to the unjittered reference, filter the jitter waveform with a 32 kHz high-pass filter and measure the peak-to-peak jitter value. Then, subtract the value with the filtered Master Mode Jitter without TX_TCLK jitter.

11.2.1 Jitter Slave Mode Unfiltered Tests

Configure the DUT to output the Test Mode 3 signal (Master) and compute the jitter on the Slave output at MDI relative to the unjittered reference. Subtract unfiltered Slave with unfiltered Master without TX_TCLK jitter. The test result is for informative purpose.

11.2.1.1 Algorithm

This section discusses the algorithm for measuring the unfiltered Slave mode jitter without access to the TX_TCLK of the DUT. This test is carried out while the DUT is operating in the Slave timing mode without the existence of a link partner. The only requirement for the test proposed in reference is this test must only be done after the Jitter Master unfiltered without TX_TCLK test has been run on the signal pair which you are concerned.

The algorithm proceeds as follows:

(1) Verify if the Jitter Master unfiltered test has been run prior to this test.

(2) Capture a long record of the signal at MDI.

(3) Compute ideal clock instants.

(4) Compute the unfiltered jitter on the Slave output at MDI relative to an ideal unjittered reference and record as unfiltered Slave.

(5) Subtract unfiltered Slave with unfiltered Master without TX_TCLK jitter and accumulate the jitter

histogram with each new acquisition until 100ms to 1 second data has been analyzed.

(6) The peak-to-peak value over the entire multi-acquisition jitter population is recorded as the unfiltered Slave without TX_TCLK jitter.

11.2.1.2 Test Environment and Connectivity

Test environment and connection for jitter tests without TX_TCLK when DUT is in slave mode, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

11.2.1.3 Test Procedure

(1) Configure the DUT to output Test Mode 3 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter Without TX_TCLK** > **Jitter Slave Mode Unfiltered (IEEE802.3-2018, 40.6.1.2.5)** .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal between 100ms to 1 second length signal. After finishing the tests will output the test results.

11.2.2 Jitter Slave Mode Filtered Tests

Without access to TX_TCLK on both Master and Slave, compute the jitter slave mode filtered on the DUT output at MDI relative to the unjittered reference, filter the jitter waveform with a 32 kHz high-pass filter and measure the peak-to-peak jitter value and subtract the filtered Slave jitter with the filtered Master jitter. The test result is for informative purpose.

11.2.2.1 Algorithm

This section discusses the algorithm for measuring the filtered Slave mode jitter without access to the TX_TCLK of the DUT. This test is carried out while the DUT is operating in the Slave timing mode without the existence of a link partner. The only requirement for the test proposed in reference is this test must only be done after the Jitter Master filtered without TX_TCLK test has been run on the wire pair which you are concerned.

The algorithm proceeds as follows:

(1) Verify if the Jitter Master filtered without TX_TCLK test has been run prior to this test.

(2) Capture at least 100,000 edges of the signal at MDI in one long record.
(3) Compute the jitter waveform of the signal at MDI relative to an unjittered reference and filter the jitter waveform with a 32kHz high-pass filter to produce a filtered Slave jitter waveform.
(4) Subtract filtered Slave with filtered Master without TX_TCLK jitter and record the peak-to-peak value as the filtered Slave jitter without TX_TCLK.

11.2.2.2 Test Environment and Connectivity

Test environment and connection for jitter tests without TX_TCLK when DUT is in master mode, please refer to <5.1 Test Environment and Connectivity Without Disturber>.

11.2.2.3 Test Procedure

(1) Configure the DUT to output Test Mode 3 signal.
(2) In **Test Select** label to select the test items, the step is **Test Select** > **Jitter Without TX_TCLK** > **Jitter Slave Mode Filtered (IEEE802.3-2018, 40.6.1.2.5)** .
(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), edge and measure time and in the **Configure** tab for the DUT test pair.
(4) Check the correctness of the test environment setup in the **Connect** tab.
(5) Click **Run Test** .
(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.
(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal for at least 100k edges. After finishing the tests will output the test results.

11.2.3 Test Results Reference

The reference result of Jitter Slave Mode filtered without TX_TCLK is shown as Figure 11-3. The waveform details are shown as Figure 11-4.

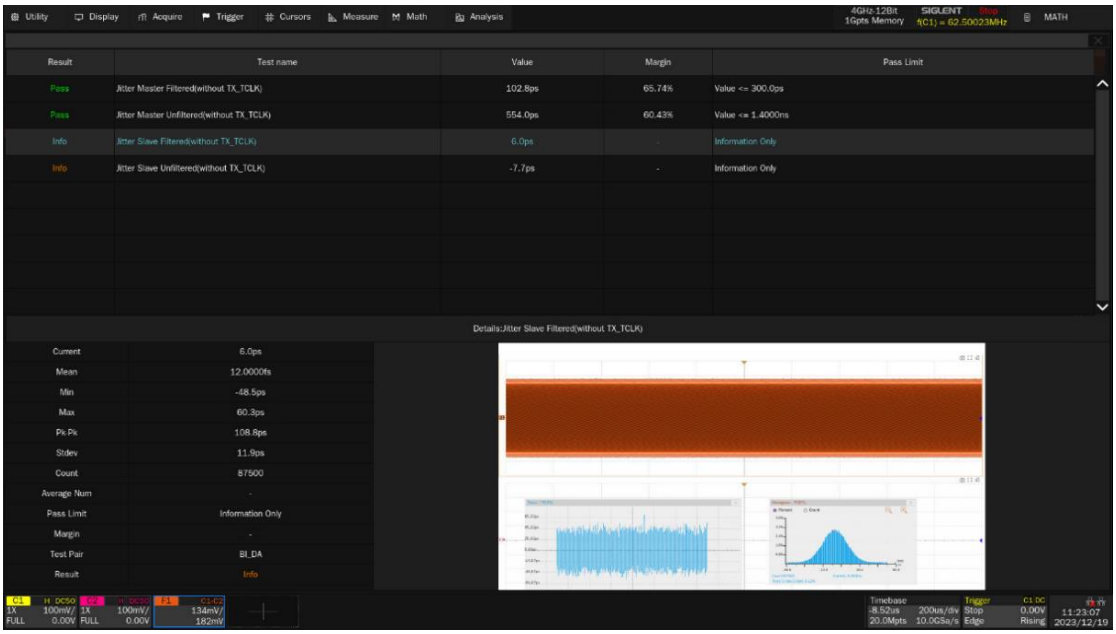


Figure 11-3 Reference results of Jitter Slave Mode Filtered Without TX_TCLK

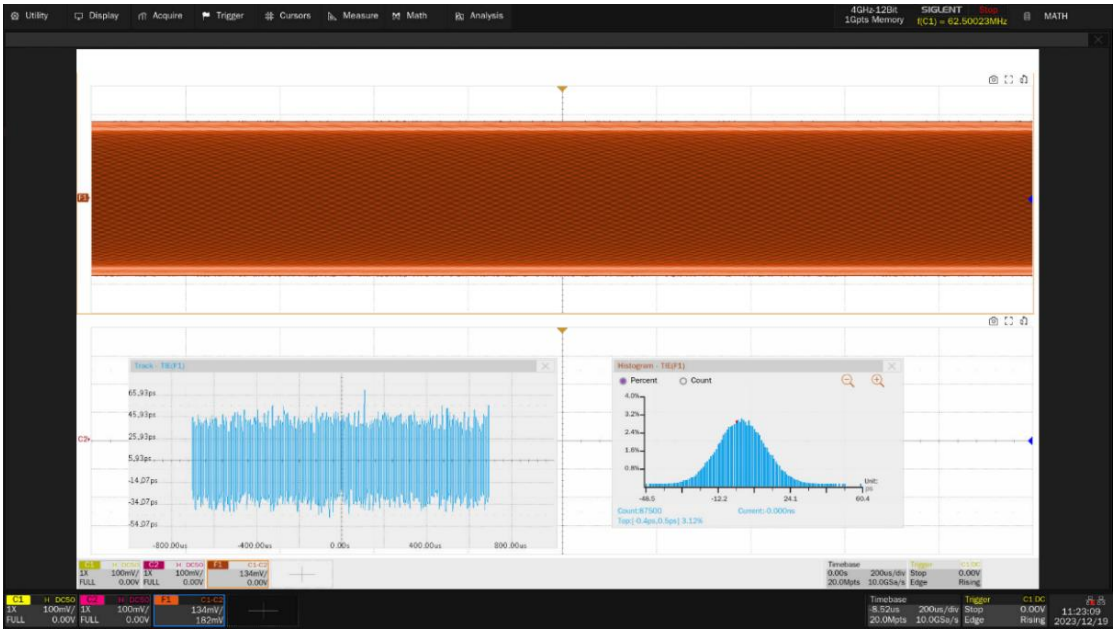


Figure 11-4 Waveform details of Jitter Slave Mode Filtered Without TX_TCLK

The reference result of Jitter Slave Mode unfiltered without TX_TCLK is shown as Figure 11-5. The waveform details are shown as Figure 11-6.

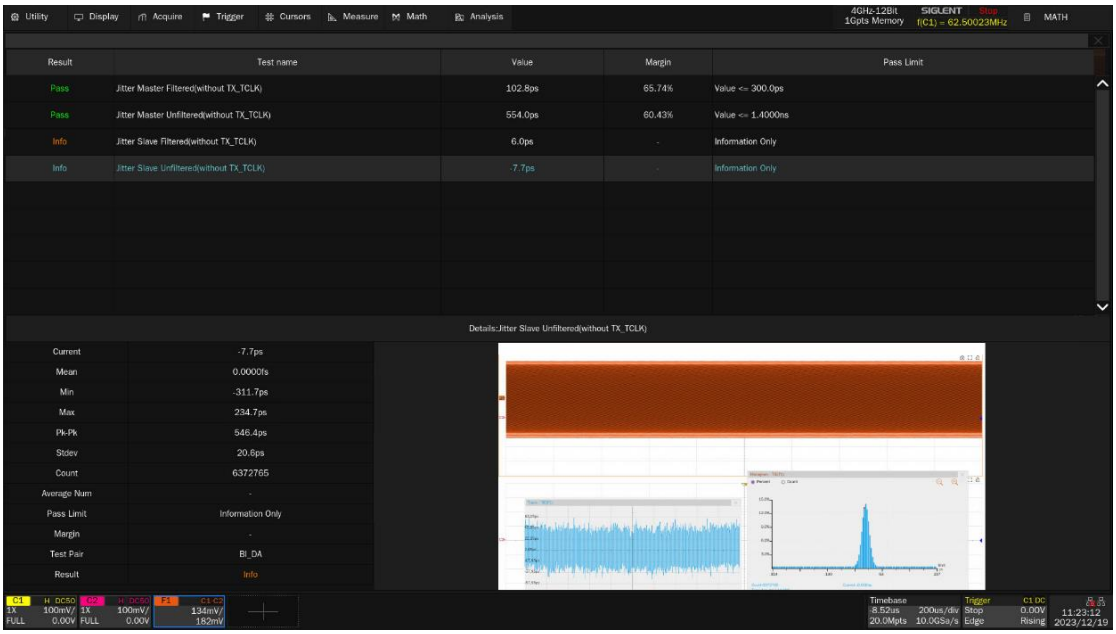


Figure 11-5 Reference results of Jitter Slave Mode Unfiltered Without TX_TCLK

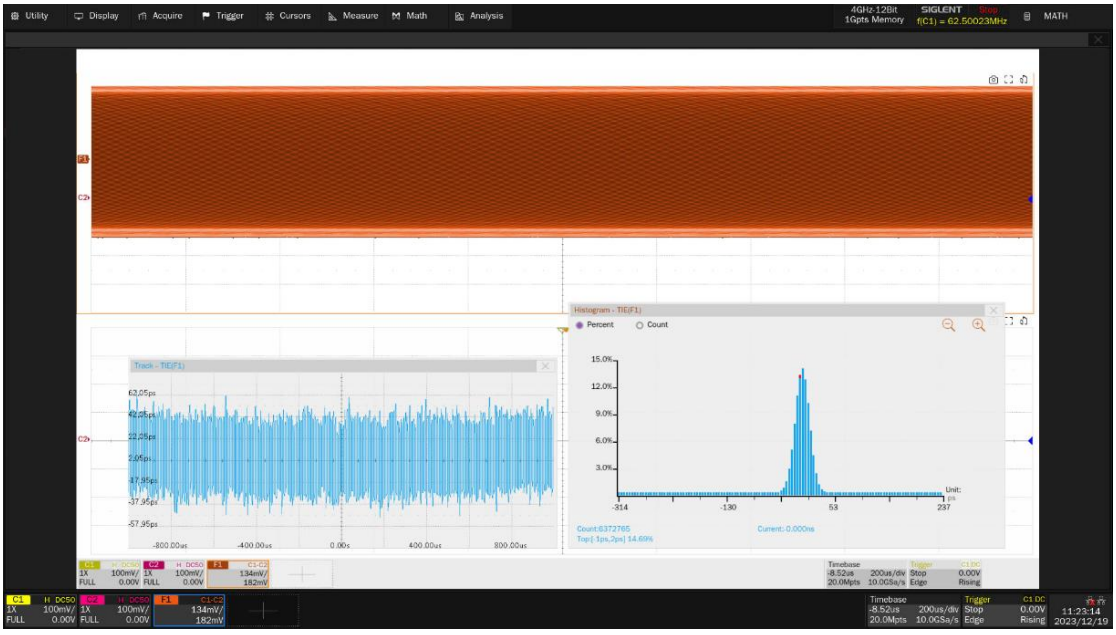


Figure 11-6 Waveform details of Jitter Slave Mode Unfiltered Without TX_TCLK

12 MDI Return Loss Tests

12.1 Standard Reference

According to the IEEE802.3-208, Subclause 40.8.3.1, differential impedance at the MDI for every transmit / receive channel shall be within the specification.

The MDI return loss tests requires the use of a vector network analyzer to test the MDI port.

To complete the test, the DUT is required to set in output Test Mode 4 signal (Master timing mode).

12.2 Algorithm

IEEE802.3-2018, Subclause 40.8.3.1 standard reference describes all the transmit / receive channel return loss specifications for a 1000 BASE-T device at the physical medium attachment (PMA) sublayer to Media Dependent Interface (MDI). The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100Ω ± 15% is attenuated, relative to the incident signal, at least 16dB over the frequency range of 1.0MHz to 40MHz and at least 10-$20\log_{10}(f/80)$ dB over the frequency range 40MHz to 100MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

12.3 Test Environment and Connectivity

For the MDI return loss test, the VNA needs to be calibrated before the return loss test, after calibration the S11 test is performed.

12.3.1 Calibrating the VNA

Steps for VNA calibration is shown as follows:

(1) On the test fixture, using two SMA cables with equal length to connect the J47 and J52 connectors on section ② to the corresponding signal pair(DA, DB, DC, DD) being tested on section ⑥.

(2) Use a SMA cable to connect one port on VNA to J48 connector on section ② of the test fixture.

(3) Connect the other unused test points on section ⑥ of the test fixture to 50Ω terminators.

(4) Using a USB cable to connect the USB Host port on the oscilloscope to the USB Device port of the VNA.

(5) On the test fixture, use a short UTP cable to connect J46 connector on section ⓪ to J27 on section ⑥.

(6) On **Test Select** label, click **Common** -> **MDI Return Loss (IEEE802.3 40.8.3.1)**. On the **Configure** label, click **Test Setup** -> **Return Loss** -> **Connect Test** , the will detect the VNA connection status, if the VNA is detected, then the VNA's Model Name will

appear, and the oscilloscope will automatically carry out the VNA setting (automatically setting only supports Siglent's VNA). The following is a list of VNA setup:

- Set the measurement type (Meas) to Return Loss (e.g., S11);
- Set the start frequency to 1 MHz;
- Set the stop frequency to 100 MHz;
- Set the IF bandwidth to 100Hz;
- Set the number of scan points to 500;
- Enables continuous scanning.

(7) Click **VNA Port Select:** to select the VNA port being used, Click **Open** to perform Open calibration.

(8) For Short and Load calibration, change the short UTP cable connection and then click **Short** and **Load** in the **Configure** label to perform calibration respectively.

VNA calibration environment is shown as Figure 12-1.

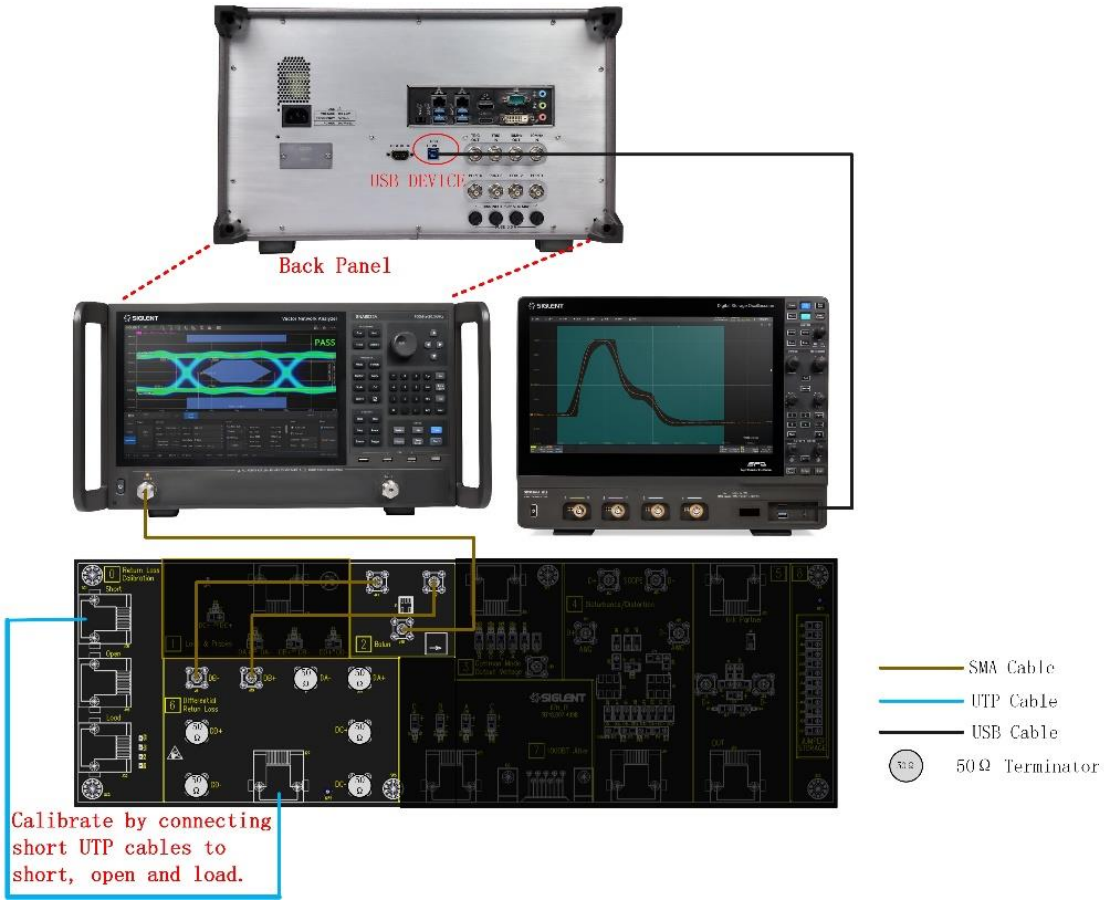


Figure 12-1 Calibration of VNA

12.3.2 Test Procedure for MDI Return Loss

MDI return loss for the DUT is performed as follows:

(1) Configure the DUT to output the Test Mode 4 signal (Master timing mode).

(2) On the test fixture, use two SMA cables with equal length to connect the J47 and J52 on section ② to the corresponding signal pair being test on section ⑥.

(3) Using a SMA cable to connect one port of VNA to J48 connector on section ② of the test fixture.

(4) Connect the other unused test points on section ⑥ of the test fixture to 50Ω terminators.

(5) Using a USB cable to connect the USB Host port on the oscilloscope to the USB Device port of the VNA.

(6) Connect the DUT to the J27 connector on section ⑥ of the test fixture by using a short UTP cable.

(7) On the Oscilloscope Click **Run Test** , and click **Run Test** when the pop-up window appears. The oscilloscope will automatically acquire the return loss data tested by the VNA and plots the curve, and outputs the test result.

Return loss test environment for DUT MDI is shown as Figure 12-2.

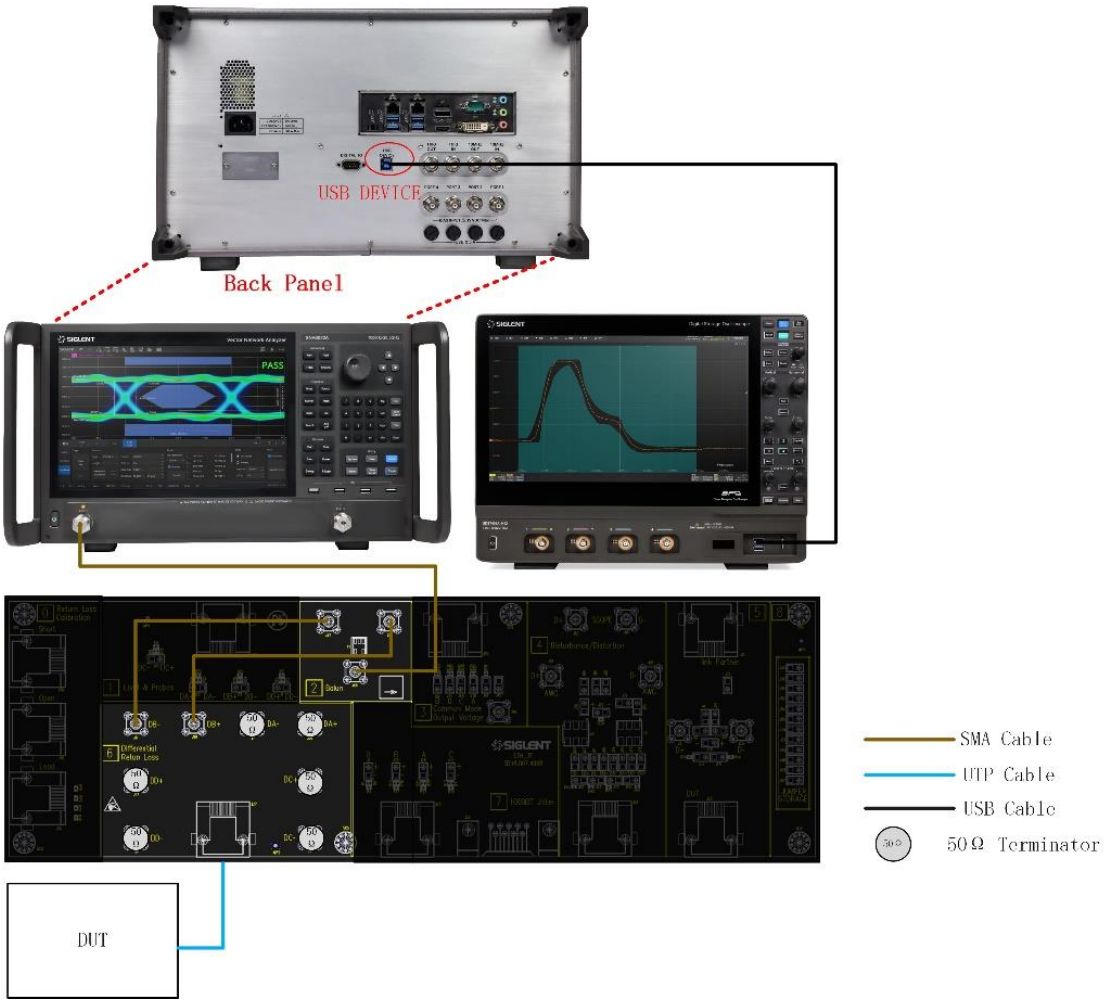


Figure 12-2 Test Environment of Return Loss

12.4 Test Results Reference

The test result reference of DUT MDI Return Loss DUT is shown as Figure 12-3.

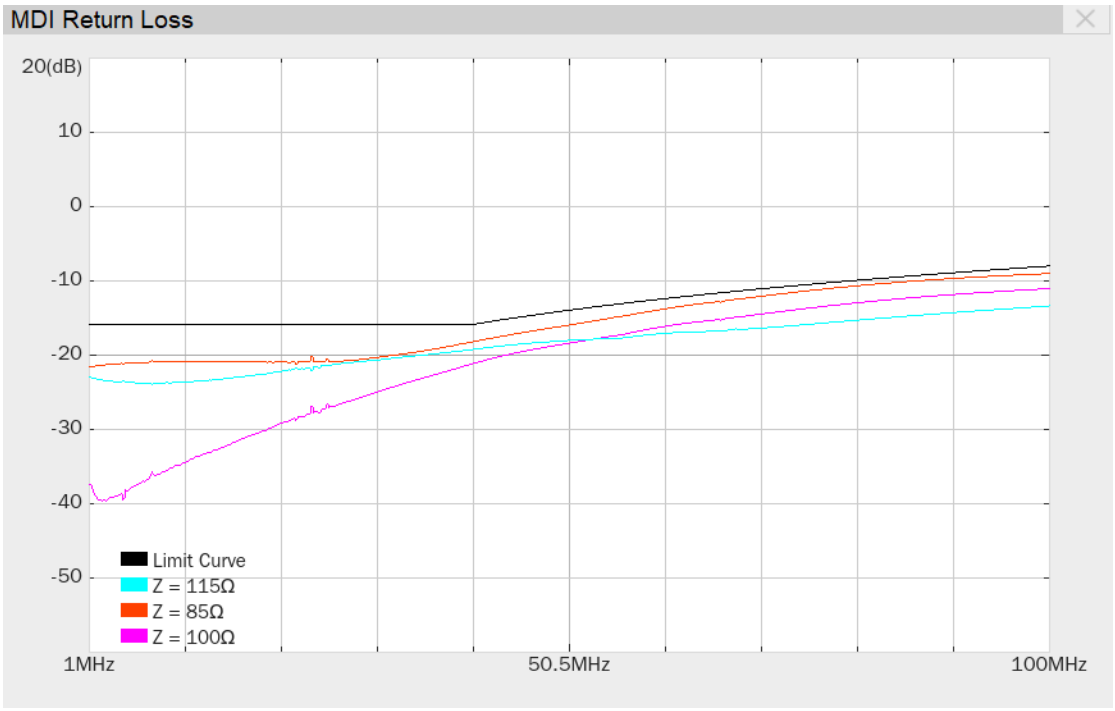


Figure 12-3 Reference results of MDI Return Loss

13 MDI Common-mode Output Voltage Tests

13.1 Test Waveform and Standard Reference

When DUT is configured to output Test Mode 4 signal, according to the standard reference IEEE802.3-2018, Subclause 40.8.3.3, the magnitude of the total common-mode output voltage, Ecm_out, on any transmit circuit, when measured as shown in Figure 13-1, shall be less than 50 mV peak-to-peak when transmitting data at frequencies above 1 MHz .

The test waveform is shown in Figure 13-2 for Test Mode 4 at DUT MDI.

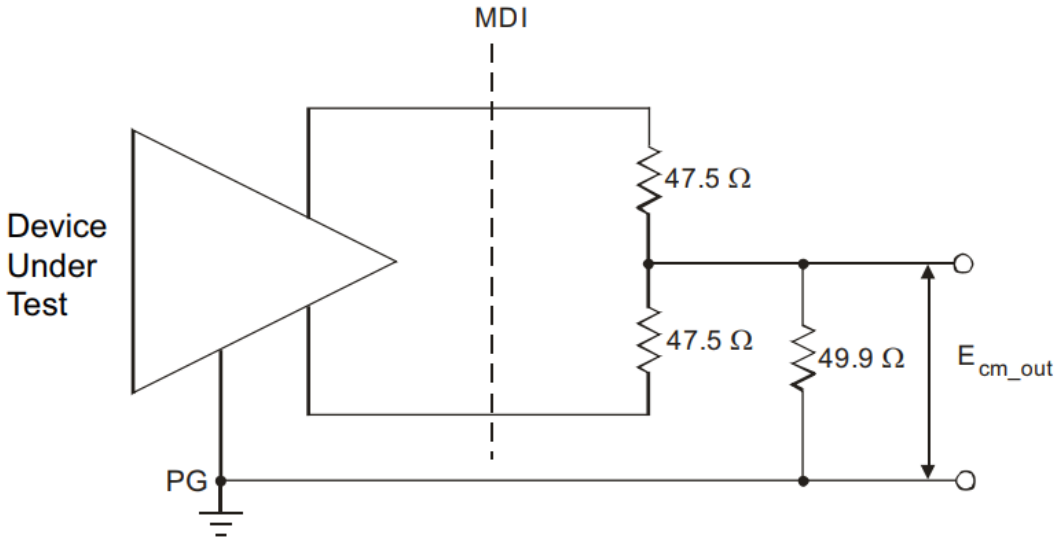


Figure 13-1 Test circuit for Common-mode output voltage

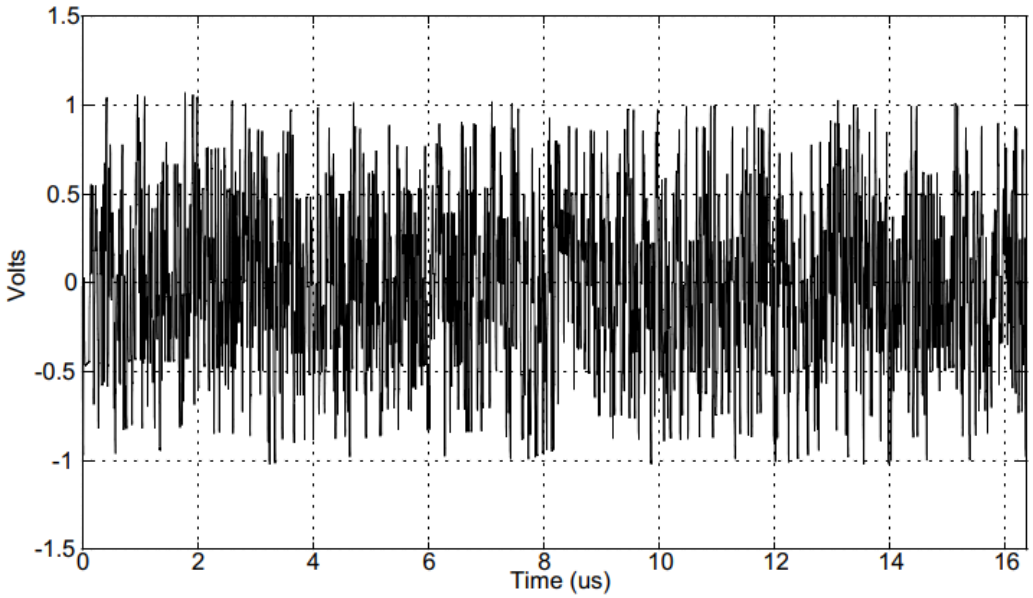


Figure 13-2 Test waveform for Test Mode 4

13.2 Algorithm

The common-mode output voltage tests require the DUT to send out a test mode 4 waveform. The oscilloscope captures the waveform over a period of time, measures the maximum and minimum values of the waveform, and subtracts the maximum value from the minimum value to obtain the maximum peak-to-peak value as the test result of the common mode output voltage. The standard requires that the maximum peak-to-peak value of the common mode output voltage is less than 50mV.

13.3 Test Environment and Connectivity

The connection for using SMA cable is shown as Figure 13-3, the connection is as follows:

(1) Connect the DUT to the J55 connector on section ③ of the test fixture by using a short UTP cable.

(2) Connect the J40 on section ③ of the test fixture to one input channel of the oscilloscope by using an SMA cable.

(3) Connect the ground point of the DUT to the ground point (J85 or J86) on the fixture with a SMA cable.

(4) Depending on the signal pair being tested, install a jumper to the corresponding connector, which is J36(Pair A), J39(Pair B), J45(Pair C), J51(Pair D).

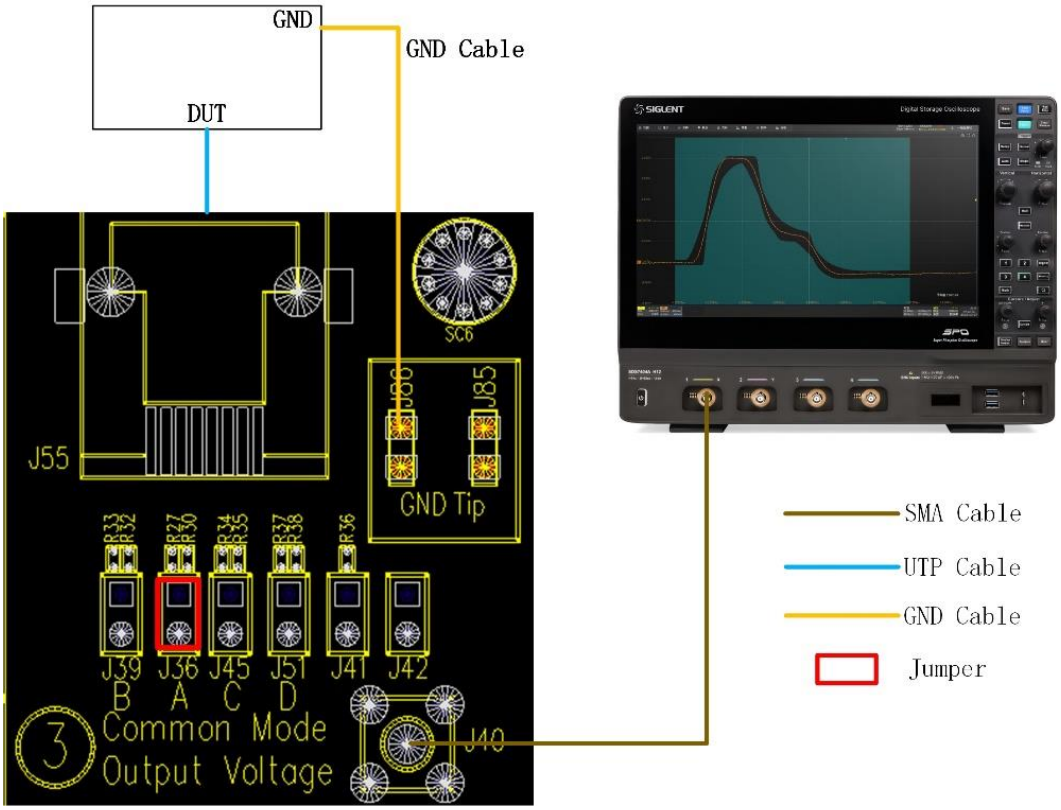


Figure 13-3 SMA cables connection in Common-mode Output Voltage

13.4 Test Procedure

(1) Configure the DUT to output Test Mode 4 signal.

(2) In **Test Select** label to select the test items, the step is **Test Select** > **Common** > **MDI Common-mode Output Voltage (IEEE802.3-2018, 40.8.3.3**) .

(3) Set the probe type (differential probe or single-ended input), input channel data, Pair ID (Pair A/B/C/D), measure time in the **Configure** tab for the DUT test pair.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the oscilloscope will configure the correct trigger level to capture the signal, and process the signal between 10ms to 100ms. After finishing the tests will output the test results.

13.5 Test Result Reference

The test result reference of MDI common-mode output voltage is shown as Figure 13-4. The details of the test waveform are shown as Figure 13-5.

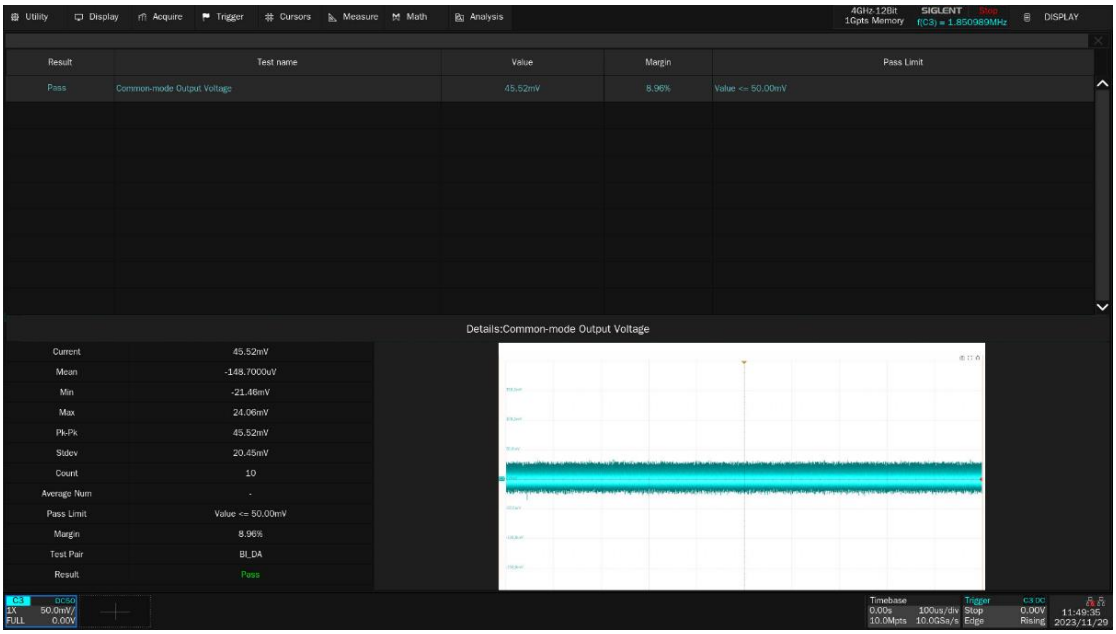


Figure 13-4 Test result reference of MDI common-mode output voltage

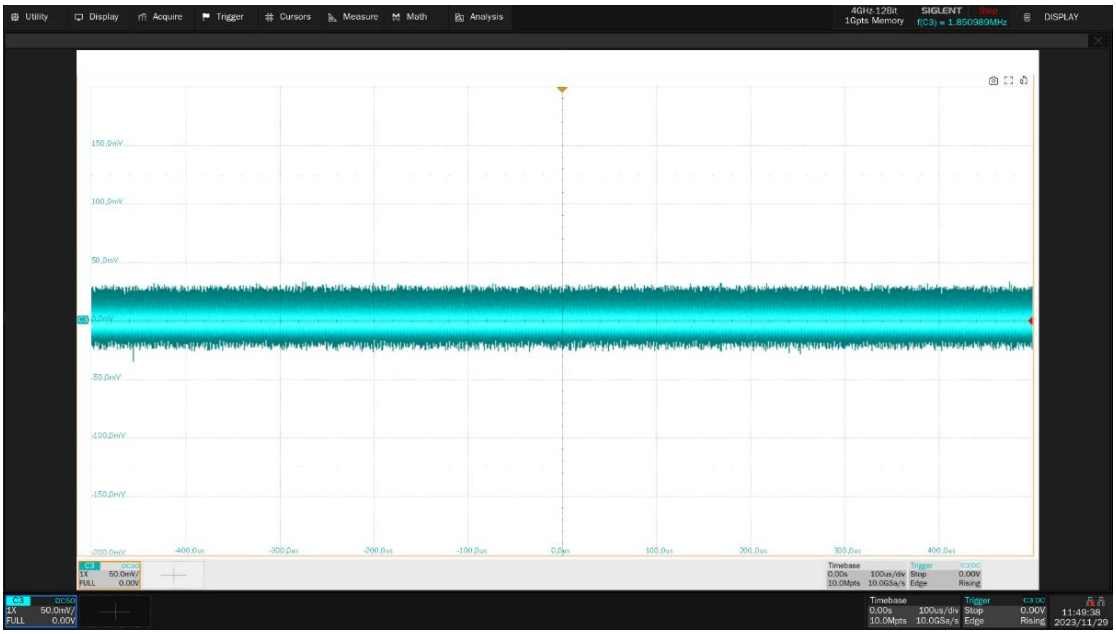


Figure 13-5 Test waveform details of common-mode output voltage

About SIGLENT

SIGLENT is an international high-tech company, concentrating on R&D, sales, production and services of electronic test & measurement instruments.

SIGLENT first began developing digital oscilloscopes independently in 2002. After more than a decade of continuous development, SIGLENT has extended its product line to include digital oscilloscopes, isolated handheld oscilloscopes, function/arbitrary waveform generators, RF/MW signal generators, spectrum analyzers, vector network analyzers, digital multimeters, DC power supplies, electronic loads and other general purpose test instrumentation. Since its first oscilloscope was launched in 2005, SIGLENT has become the fastest growing manufacturer of digital oscilloscopes. We firmly believe that today SIGLENT is the best value in electronic test & measurement.

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